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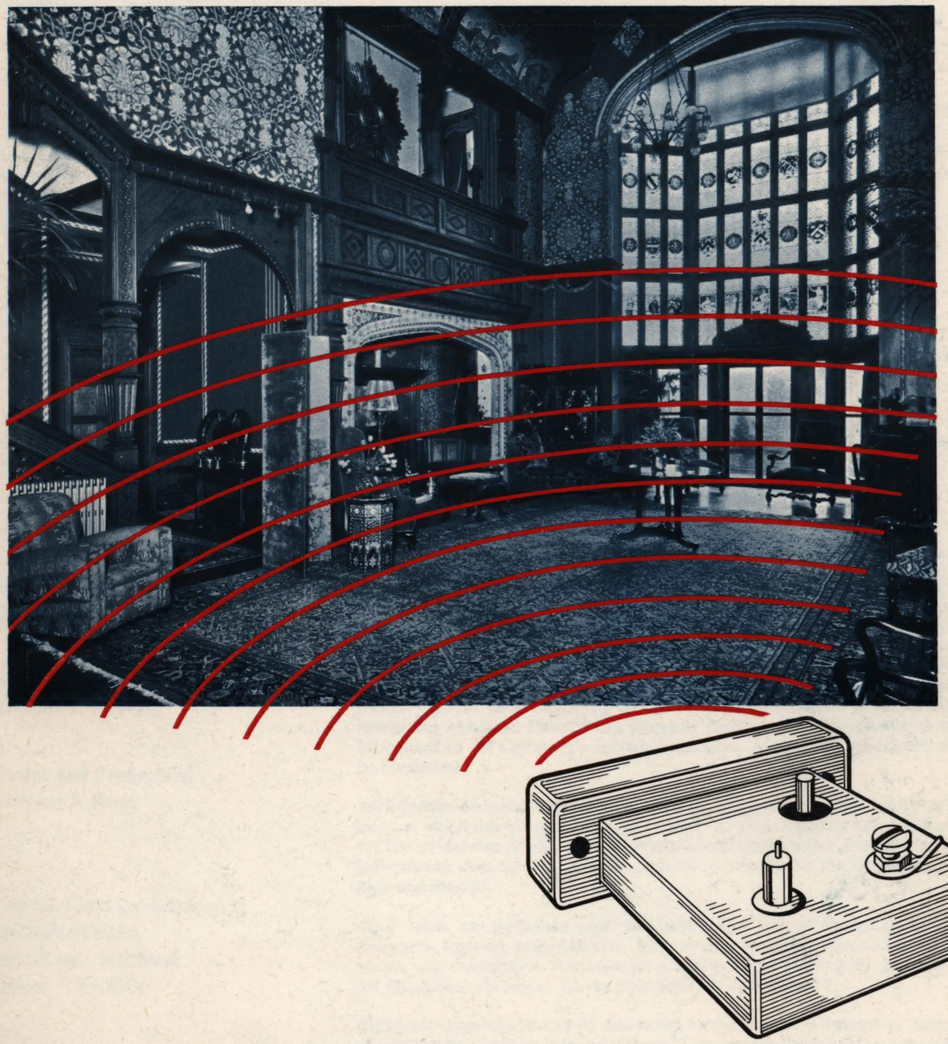

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Cover picture:
Microwave doppler radar alarm systems are ideal for use in many security applications. An alarm system using the CL8960 or CL8920 doppler radar modules is described in detail in this issue.

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Switched-mode field deflection for 20AX television using TDA2600

A.J. TERRY*
Mullard Central Application Laboratory

A switched-mode field timebase suitable for scanning the 110° 20AX colour picture tube is described. The circuit is capable of being easily adapted for other tv systems.

The total circuit power is 13W compared with a typcial figure for a class B circuit of 22W. As a result of the low dissipation in the output devices, it has been possible to integrate the circuit including the output stage as the TDA2600. This leads to a compact circuit, particularly because of the reduction in heatsink area. The circuit is outstandingly safe against the effects of picture tube flashover.

INTRODUCTION

The use of integrated circuits in television receivers has now extended to most small-signal areas, and it is mainly in the high-voltage and high-power areas where discrete semiconductor devices must still be used.

One area which has not been fully integrated is the complete field timebase for full-performance 110° colour receivers. Integrating the sawtooth generator and the shaping and driver stages is no problem, but with the output stages operating in class B the relatively large dissipation has precluded the use of an economic integrated solution.

Operating the output stage in a switching mode reduces the dissipation to less than 5W from at least 12W for class B (with 20AX) and enables the output devices to be incorporated in an integrated circuit package with the inherent advantage of reliability, space saving, and ease of servicing.

*The TDA2600 was developed jointly by B.E. Attwood, formerly of the Mullard Central Application Laboratory, and A.J. Terry.

PRINCIPLES OF SWITCHED-MODE FIELD DEFLECTION

The principle of switched-mode operation can be seen from Figs. 1a and 1b. If a high-frequency pulse train is applied to a suitable lowpass filter, the output will be the average value of the waveform at any instant. Thus if the pulse train is of constant and equal mark-space ratio as in Fig. 1a, the output will be a d.c. voltage equal to half the peak amplitude of the switching waveform.

Consider now what happens when the pulse width is altered as in Fig. 1b. Since the lowpass filter will give the average value of the waveform at any instant, the output at the start of the pulse train will be near to the positive supply voltage and at the end it will be zero. With the form of pulse-width variation shown in Fig. 1b, the resultant output will be a decreasing ramp, and, if these pulses are capable of providing high currents, a sawtooth of sufficient power to drive a field deflection coil will be available.

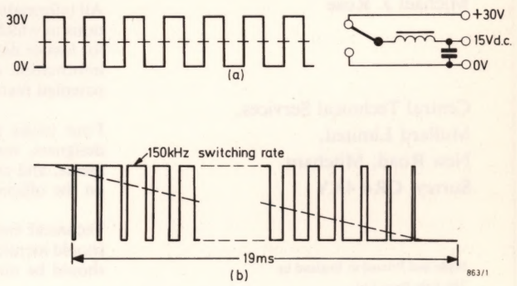


Fig. 1 — Principle of switched-mode operation

The analogue-to-digital conversion is achieved by use of a high-frequency triangle waveform and a differential amplifier: one side of this amplifier is connected to the triangle generator and the other side to the 50Hz sawtooth waveform source. A triangle is used because it provides the required linear modulation and may be easily generated.

The actual mechanism of modulation can be described by reference to Fig. 2a which shows the two waveforms applied to opposite sides of the differential amplifier, the shaded area representing conduction of the output stage of the modulator.

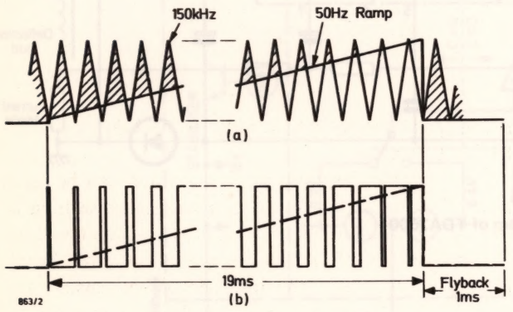


Fig. 2 — Conversion of 50Hz ramp to pulse-width modulated train

At the start, the shaded area is wide so that the transistor conduction period is long, producing a low average value of output voltage (Fig. 2b); halfway through scan the waveform has a 1:1 mark-space ratio and the average value is mid-way; at the end, the system just conducts narrowly, resulting in a short conduction period with a high average value of output voltage. The broken line represents the average value of the waveform. The switching waveform is then applied to the power stage, and the high-load switching waveform is applied to a lowpass filter which reconstitutes the original 50Hz sawtooth component for driving the deflection coils.

For the flyback period, once this has been initiated by the ramp generator, the system is locked in one state as a result of the action of the feedback loop and the output voltage is effectively clamped to the supply positive rail until the current in the deflection coils has fully reversed. Thus for a period of approximately 1ms in every 20ms the system does not switch at high frequency.

Conventional class B clamped-flyback operation, particularly when there is a high ratio of flyback to scan voltage, can result in considerable power loss because of the extra supply voltage requirement, but for a pulse-width modulated switching system which has a substantially constant efficiency, little dissipation penalty is incurred.

FUNCTIONS OF THE INTEGRATED CIRCUIT TDA2600

The functions of the TDA2600 can be divided into seven blocks as shown in Fig. 3. An appropriate configuration has been chosen to permit a single circuit block and timing network to perform the functions of field oscillator and ramp generator, while still providing independent controls for frequency, height, and linearity. This circuit requires negative-going synchronising pulses, and so a sync inverter is provided to accommodate positive-going signals.

The positive-going ramp is externally mixed with the negative-going signal from the deflection current sensing resistor, and the resulting feedback error signal is applied to the pre-amplifier input at pin 7. The modulator compares the analogue signal from the pre-amplifier output (pin 5) and the high frequency signal from the triangle generator output (pin 4), and delivers a width-modulated pulse train to the output stage.

The power output stage contains a pair of transistors which can each handle currents in excess of 2A, but it is more economical for the energy-recovery diodes to be external to the chip. The high level switching waveform thus produced is applied to a lowpass LC filter to recover the 50Hz analogue signal which, with a capability of at least 4A pk-pk, is suitable for nearly all types of deflection coils.

The constituents of the individual circuit blocks are shown in some detail in Fig. 4 and described in the sections below.

Field oscillator/ramp generator

A positive-going ramp is produced at pin 12 by the external timing resistor charging the split timing capacitor. Normally, this resistor will be taken to a suitable scan-rectified supply rail so that the vertical amplitude tracks with the line amplitude to maintain a constant picture aspect ratio. To give good height stability the resistor should at least be of a carbon film type, and in some cases (if, for example, high ambient temperatures may be encountered) a high-stability type may be advantageous.

It can be seen in Fig. 4 that when the voltage at pin 12 exceeds that at pin 11 by approximately 1.2V (that is, $2 \times V_{BE}$), the ramp generator comparator switches (because 'E' becomes greater than 'F') and a much higher current (approximately 5mA) is drawn into pin 12, thus discharging the timing capacitors until the voltage has fallen to approximately 1.2V above earth (pin 9): the circuit then restores; that is, it returns to its

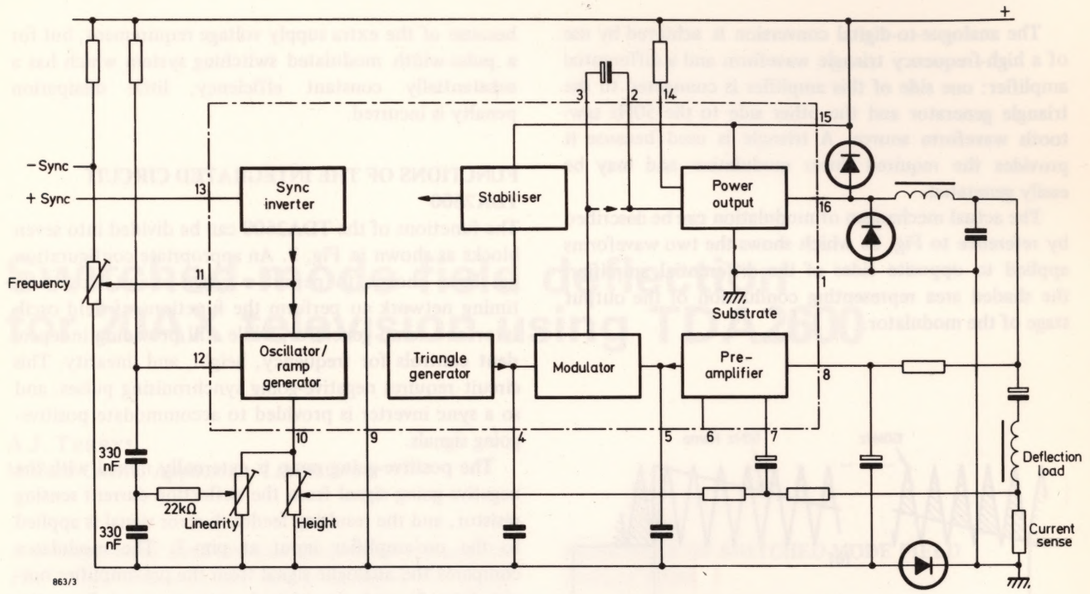


Fig. 3 — Block diagram of TDA2600

initial scanning mode. The variable potential divider on pin 11 provides a means for adjusting the free-running frequency without affecting the amplitude when synchronised, and if this chain is connected to the same supply rail as the timing resistor, variations of the supply do not significantly alter the free-running frequency.

The high-impedance waveform at pin 12 passes through a chain of complementary emitter-followers and appears with much lower impedance at pin 10. The waveforms are therefore very similar in amplitude and d.c. level during scan, but an internal clamp operates at the start of flyback to rapidly initiate the flyback state in the subsequent circuitry.

The linearity control feeds an adjustable amount of the ramp generator output waveform to the integrating network consisting of the 22kΩ resistor and the lower 330nF timing capacitor (Fig. 3). Integration of the ramp produces a parabolic waveform with 'troughs' downwards, and this is coupled via the upper 330nF timing capacitor to the input at pin 12, thus modifying the ramp to one which increases in steepness as the scanning cycle progresses. This compensates for the 'roll-off' in gradient due to the finite ramp aiming voltage and the effects of the various a.c. couplings in the complete system.

The amplitude of the ramp waveform fed forward to the pre-amplifier is adjusted by means of a low-impedance potentiometer, providing good picture height stability with variations of temperature and humidity.

The oscillator is synchronised by using the sync pulse to lower the upper threshold voltage at pin 11. If the ramp has already passed the lowered threshold, flyback is initiated immediately. During most of the scan period, however, the ramp voltage is less than the lowered threshold, and so spurious sync pulses during this period have no effect.

If negative-going sync pulses are available, they may be applied directly to the frequency control network via an appropriate resistor to give the desired pull-in range. The pull-in range is equal to the percentage change in voltage (relative to the d.c. level) at pin 11 produced by the sync pulse. In general it is not necessary to a.c. couple the pulse, provided that when optimising the frequency control network values, allowance is made for any d.c. offset introduced.

Because of the very high input impedance of the sync inverter input (pin 13), it is recommended that when negative-going sync is being employed, pin 13 should be taken to earth (preferably pin 9) to prevent any leakage currents or 'pick-up' disturbing the oscillator.

Sync inverter

When positive-going sync pulses are to be used, the sync inverter internally connected between pins 13 and 11 is employed. As shown in Fig. 4, pin 13 is the input to a darlington emitter-follower which feeds a 'current

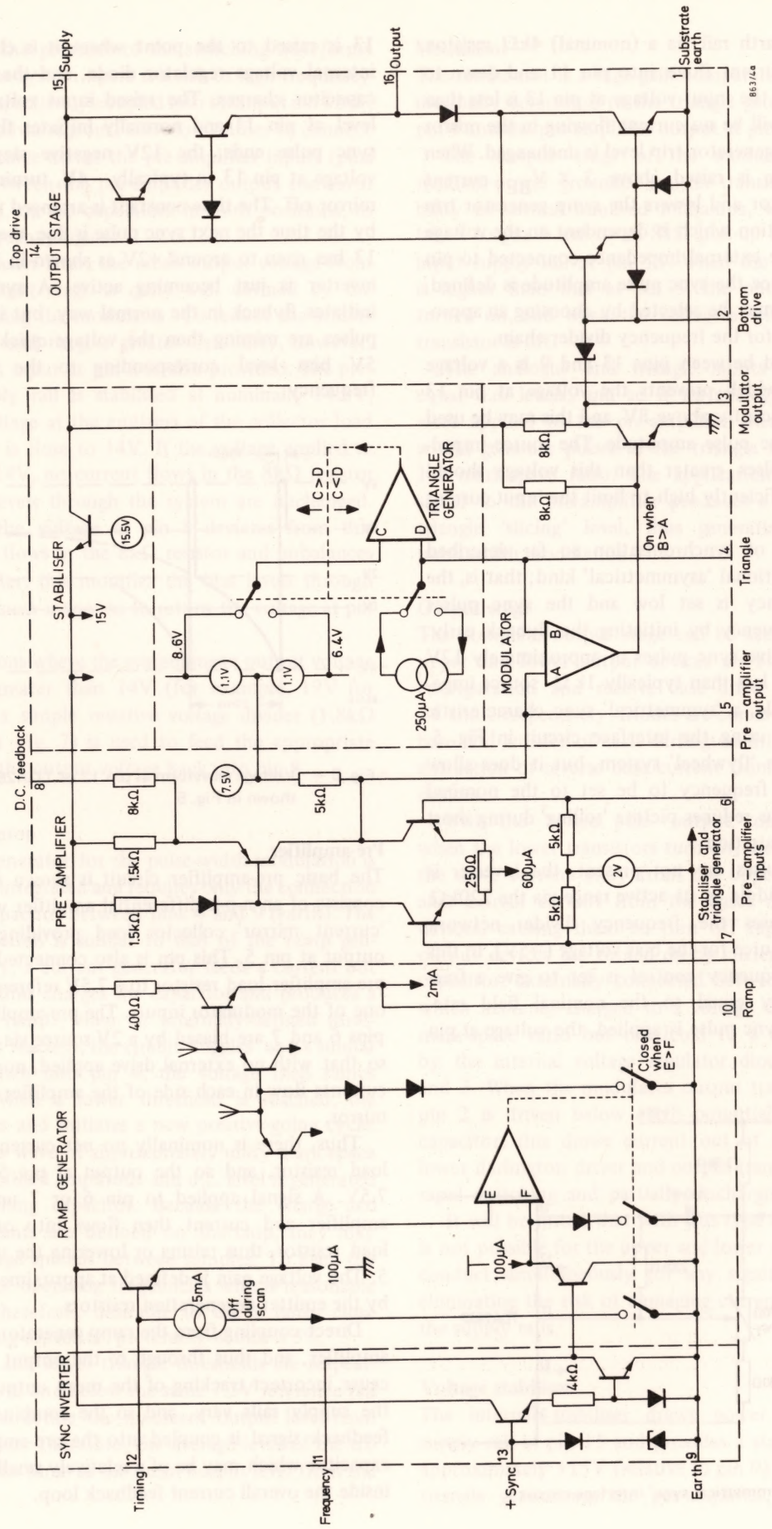


Fig. 4 — Schematic functions of TDA2600 chip

mirror' on the earth rail via a (nominal) 4kΩ resistor. The 'mirrored' current flows into pin 11 and down to earth at pin 9. If the input voltage at pin 13 is less than $3 \times V_{BE}$, there will be no current flowing in the mirror and so the ramp generator trip level is unchanged. When the input voltage is raised above $3 \times V_{BE}$, current flows in the mirror and lowers the ramp generator trip level by a proportion which is dependent on the voltage at pin 13 and the external impedance connected to pin 11. Therefore, once the sync pulse amplitude is defined, the pull-in range may be selected by choosing an appropriate impedance for the frequency divider chain.

Also connected between pins 13 and 9 is a voltage regulator diode which prevents the voltage at pin 13 from rising significantly above 8V, and this may be used to define the sync pulse amplitude. The source impedance of sync pulses greater than this voltage should preferably be sufficiently high to limit the input current to less than 5mA.

The methods of synchronisation so far described are of the conventional 'asymmetrical' kind; that is, the oscillator frequency is set low and the sync pulses increase the frequency by initiating the flyback early. However, if positive sync pulses of approximately 12V amplitude and of less than typically 1kΩ source impedance are available, a 'symmetrical' sync characteristic may be attained using the interface circuit in Fig. 5. This is not a true 'flywheel' system, but it does allow the free-running frequency to be set to the nominal field rate, and thus reduces picture 'rolling' during short breaks in synchronisation.

When sync pulses are not present, the inverter is biased near the middle of its active range via the 220kΩ resistor which uses the frequency divider network as a convenient source for the bias voltage (≃5V). In this condition the frequency control is set to give a free-running frequency equal to the nominal field rate. When a positive sync pulse is applied, the voltage at pin 13 is raised to the point where it is clamped by the internal voltage regulator diode, and the sync coupling capacitor charges. The raised input voltage lowers the level at pin 11 and normally initiates flyback. As the sync pulse ends, the 12V negative step reduces the voltage at pin 13 to typically −4V, turning the inverter mirror off. The time-constant is arranged to be such that by the time the next sync pulse is due, the voltage at pin 13 has risen to around +2V as shown in Fig. 6 and the inverter is just becoming active. A sync pulse then initiates flyback in the normal way, but if one or more pulses are missing then the voltage quickly reaches the 5V bias level corresponding to the nominal field frequency.

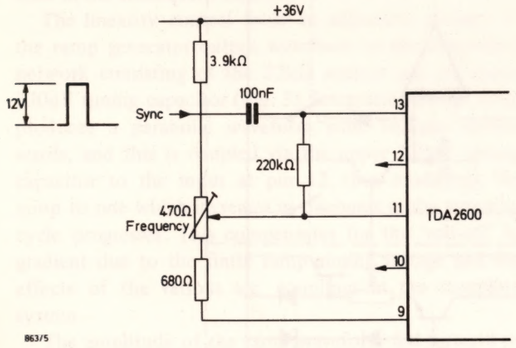


Fig. 5 — 'Symmetrical sync' interface circuit

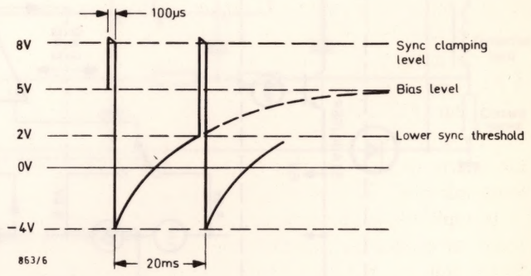


Fig. 6 — Voltage waveform at pin 13 of TDA2600 with circuit shown in Fig. 5

Pre-amplifier

The basic pre-amplifier circuit is shown in Fig. 4 and consists of an n-p-n differential amplifier with an active 'current mirror' collector load providing a push-pull output at pin 5. This pin is also connected via the 5kΩ pre-amplifier load resistor to a 7.5V reference rail and to one of the modulator inputs. The pre-amplifier inputs at pins 6 and 7 are biased by a 2V source via 5kΩ resistors so that with no external drive applied, nominally equal currents flow in each side of the amplifier and the load mirror.

Thus, there is nominally no net current flow in the load resistor, and so the output at pin 5 is biased at 7.5V. A signal applied to pin 6 or 7 unbalances the amplifier and current then flows into or out of the load resistor, thus raising or lowering the voltage at pin 5. The voltage gain is defined at approximately 15 times by the emitter degeneration resistors.

Direct coupling from the ramp generator into the pre-amplifier, and thus through to the output stage, would cause incorrect tracking of the mean output level when the supply rails vary, and so the combined ramp and feedback signal is coupled into the pre-amplifier with a capacitor which may be of a relatively small value as it is inside the overall current feedback loop.

Because of the presence of the switching waveforms elsewhere in the system, there is a risk of high-frequency signals being capacitively coupled into the input network; it is generally advantageous, therefore, either to connect a small capacitance across the pre-amplifier inputs (pins 6 and 7) or between the pre-amplifier output and earth (pins 5 and 9), or use capacitors in both positions, to reject high-frequency signals.

As will be seen later, the mean output voltage from the power output stage is quite well defined by the method of biasing the modulator. To reduce the effects of IC spreads and to give greater flexibility, however, a d.c. feedback input at pin 8 is also provided. The pre-amplifier supply rail is stabilised at nominally 14.5V, and so the voltage at the emitters of the collector load current mirror is close to 14V. If the voltage applied to pin 8 is also 14V, no current flows in the 8kΩ resistor and the bias levels through the system are unchanged. If, however, the voltage at pin 8 deviates from this value, current flows in the 8kΩ resistor and unbalances the pre-amplifier; this modifies the bias levels through the system in such a way as to return the voltage at pin 8 towards 14V.

In applications where the system mean output voltage needs to be greater than 14V (for example, 19V for 20AX coils), a simple resistive voltage divider (1.8kΩ plus 5.6kΩ in Fig. 7) is used to feed the appropriate proportion of the output voltage back into pin 8.

Triangle generator

The triangle generator for the pulse-width modulation is almost totally integrated and requires only the connection of a timing capacitor between pins 4 and 9 (earth). The mode of operation is similar to that of the ramp generator. Initially, a current generator feeds a current out of pin 4 and thus charges the capacitor and produces a positive-going ramp. When an internally-defined threshold voltage is reached, the circuit 'toggles' and a similar current is drawn into pin 4; the voltage then ramps downwards. When a lower threshold is reached, the circuit restores and initiates a new positive-going cycle. Thus a triangle wave of approximately unity mark-space ratio and of defined amplitude and d.c. level is generated across the timing capacitor. Because the charge and discharge currents are defined on the chip, they may have rather large spreads between samples. To keep the overall range of operating frequencies within reasonable limits it is, therefore, desirable to use a fairly close tolerance timing capacitor, preferably within ± 5%.

The upper and lower triangle thresholds are respectively 1.1V above and below the same 7.5V reference rail as that used to define the quiescent output level from the pre-amplifier. Therefore, the average level of the triangle wave is the same as the mean output level from the pre-amplifier.

Modulator

The modulator is a high-gain comparator with its inputs internally connected to the triangle generator output at pin 4 and the pre-amplifier output at pin 5.

The output stage of the modulator contains a medium-power grounded-emitter transistor with a capability of several hundred milliamps, with its collector taken to pin 3 and to an 8kΩ pull-up resistor from the input supply rail at pin 15. When the voltage at pin 4 is higher than that at pin 5, the output transistor is turned on, and when the voltage at pin 4 is lower, the transistor is off.

The analogue and triangle inputs have nominally equal d.c. levels, and so if no analogue (ramp) signal were applied to the pre-amplifier then the modulator would generate pulses at the triangle frequency with a 1:1 mark-space ratio. The application of an analogue signal to the pre-amplifier produces a variation of the triangle 'slicing' level, thus generating the required pulse-width modulation.

Output stage

The complete output stage can be seen in Fig. 4. The upper and lower output devices are both of darlington configuration and receive base drive current via pins 14 and 2 respectively. Diodes are connected between the base and emitter of each darlington driver to permit the extraction of reverse base current from the main power devices.

With the 'totem pole' output configuration used, when the lower transistors turn on, they not only divert the drive current away from the upper transistors, but also extract current from the bases of both of these devices, causing them to turn off rapidly. The lower output devices are turned on by current flowing in the capacitor, externally connected between pins 2 and 3, which becomes charged to a voltage dependent on the mark-space ratio but restricted to a maximum of 7V by the internal voltage regulator diode across pins 2 and 3. When the modulator output transistor turns on, pin 2 is driven below earth potential by the charged capacitor; this draws current out of the bases of the lower darlington driver and output transistors, providing rapid switching and partially discharging the capacitor.

It will be noted that with this type of output stage it is not possible for the upper and lower output devices to conduct simultaneously for any significant time, thus eliminating the risk of damaging current surges between the supply rails.

Voltage stabiliser

The internal stabiliser draws power from the main supply rail at pin 15 and provides a stabilised supply of approximately +15V (relative to pin 9) for the ramp and triangle generators, the pre-amplifier, and modulator.

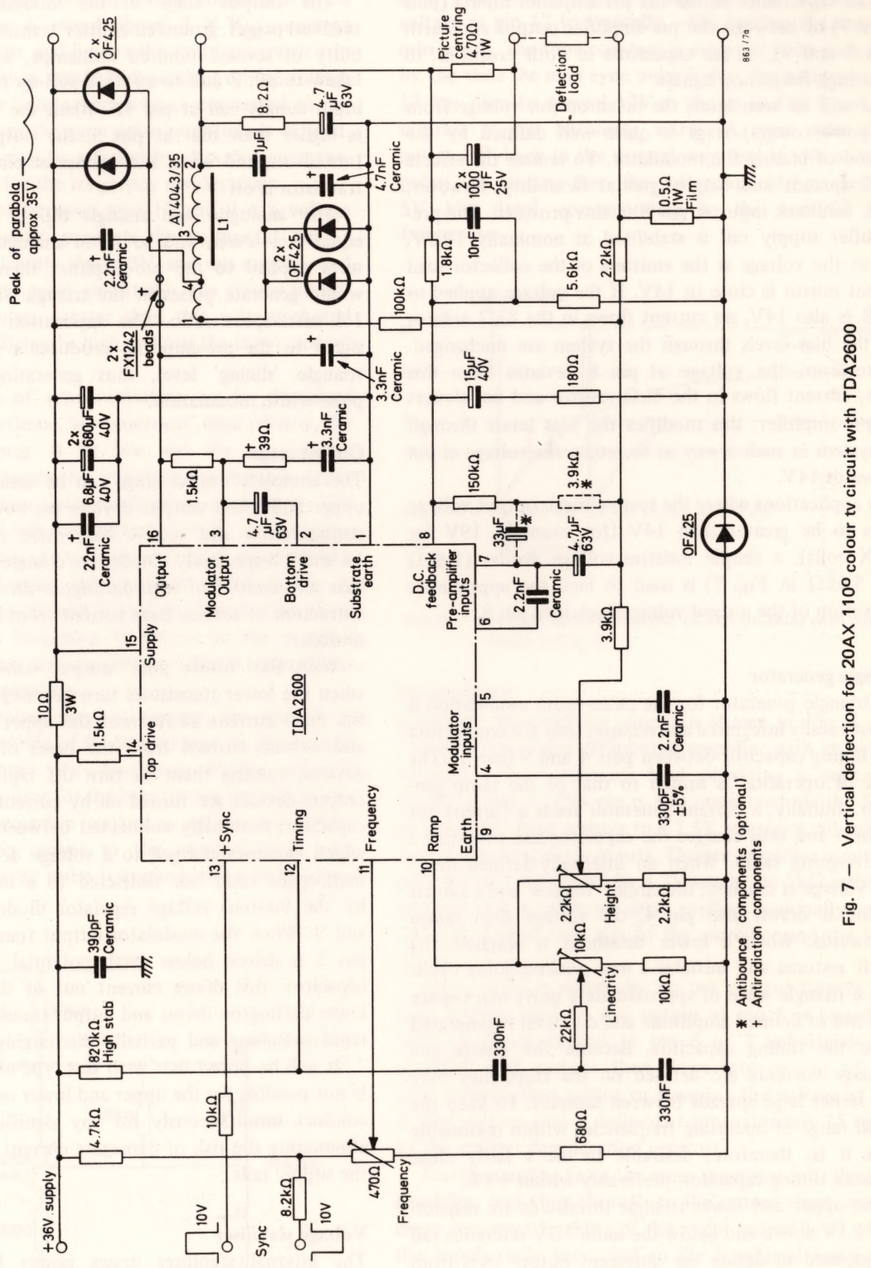


Fig. 7 — Vertical deflection for 20AX 110° colour tv circuit with TDA2600

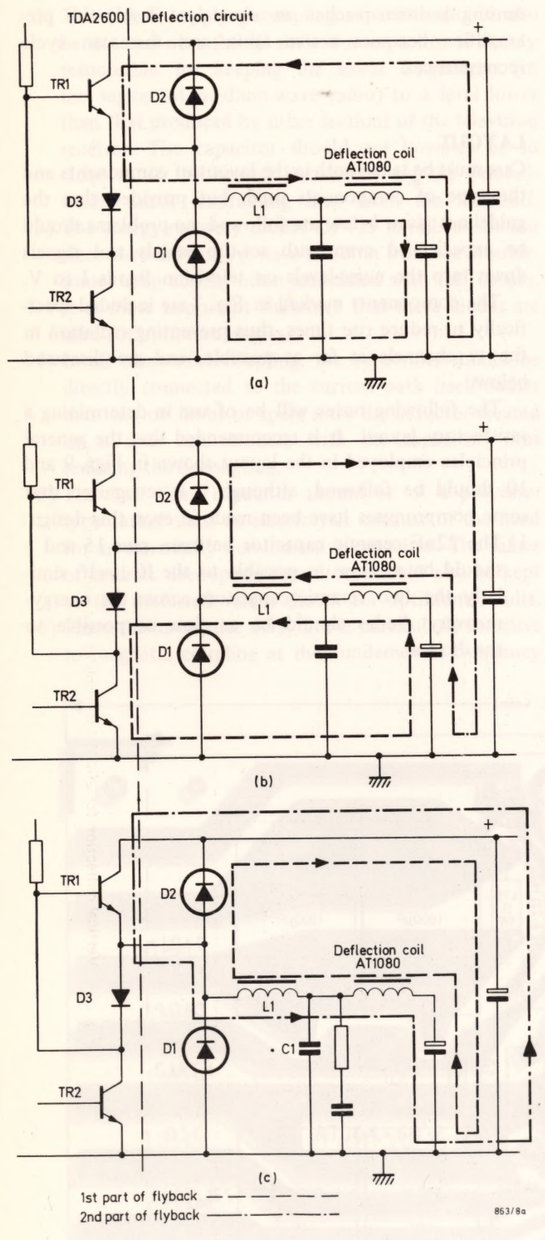


Fig. 8 — Main current flow paths during:
(a) first half of scan
(b) second half of scan
(c) flyback

For satisfactory stabilisation a drop of a few volts is required across the series transistor, and so the operational voltage at pin 15 is required to be greater than +18V at the trough of the parabolic ripple on this rail.

THE OUTPUT CIRCUIT

Circuit description

The switching waveform from pin 16 (see Fig. 7) is first shunted by a 3.3nF ceramic capacitor to earth. This capacitor slows the switching edges and is an anti-radiation measure. The waveform is then applied to two ferrite beads before being connected to the filter choke and capacitor combination. The ferrite beads are also an anti-radiation measure.

The filter inductance L_1 and the 1µF filter capacitor form a simple lowpass filter to remove switching ripple and thus to reconstitute the 50Hz sawtooth drive to the deflection coils.

The total output circuit including deflection coil has a cut-off frequency of approximately 3kHz which is quite adequate when considering the 50Hz ramp and flyback requirement.

Energy-recovery diodes are used for returning the stored energy in the inductor L_1 to the supply rails.

If the basic choke and diode output circuit shown in Fig. 3 were used, the displayed raster would show a 'bright-up' across the centre horizontal region, rather similar to crossover distortion in class B stages. This is caused by the different output stage clamping levels occurring between conduction of the output transistors, and energy recovery via the associated 'catching' diodes, and appears as a step in the switching envelope waveform at the IC pin 16, when the deflection current reverses.

This problem is overcome by the use of the tapped choke in Fig. 7, which is arranged so that the voltages developed across the small 'overwinds' just compensate for the appropriate diode and transistor voltage drops at the centre of scan.

Operation during first half of scan

During the first half of scan (Fig. 8a), TR_1 and D_1 alternately carry the load current according to whether TR_1 is saturated or cut off. When TR_1 is saturated (TR_2 is cut off), current flows via the supply rail, TR_1, L_1, and the load. When TR_1 is cut off, the energy stored in the inductor is recovered via D_1.

Although TR_2 is basically on whenever TR_1 is cut off, during the first half of scan TR_2 does not provide the load current for scanning but only acts as the switch controlling TR_1.

Operation during second half of scan

During the second half of scan it is TR_2 and D_2 that carry the load current (Fig. 8b), the current flowing via L_1, D_3, and TR_2. Whenever TR_2 is on, TR_1 is off. The energy stored in L_1 is recovered in the second half of scan by D_2 and returned to the positive supply rail.

Operation during flyback

The mode of operation is as follows. Flyback is initiated by the ramp generator which feeds a large-amplitude voltage step to the pre-amplifier input. This step, applied to the modulator, cuts off the lower output transistor TR_2 (Fig. 8c) for the whole of the flyback cycle.

As a result of the stored energy in the field coils, the voltage rises rapidly until it is clamped to the positive supply rail voltage by diode D_2. Overshoot due to the inductance of L_1 is restrained by the series CR damping network across C_1. Current continues to flow into the supply rail via D_2 until the stored energy has been recovered. Current now flows from the supply via TR_1 and increases because of the substantially fixed voltage across the deflection coils.

By this time the ramp generator has restored, and is defining a voltage level corresponding to the start of scan current. When the feedback signal from the current sensing resistor reaches an equivalent level, the pre-amplifier becomes active again and the scan cycle recommences.

LAYOUT

Care must be taken both in the layout of components and the type of components used, but provided that the guidelines given below are followed, no problems should be experienced even with set-top aerials and signals down into the noise-levels on television Bands I to V.

The components marked in Fig. 7 are included specifically to reduce rise times, thus preventing radiation in the tv channels as far as possible, and are discussed below.

The following notes will be of use in determining a satisfactory layout. It is recommended that the general principles employed in the layout shown in Figs. 9 and 10 should be followed, although it is recognised that some compromises have been made in even this design.

1) The 22nF ceramic capacitor between pins 15 and 1 should be as close as possible to the IC itself: similarly the two ceramic capacitors across the energy-recovery diodes should be as close as possible to the diodes.

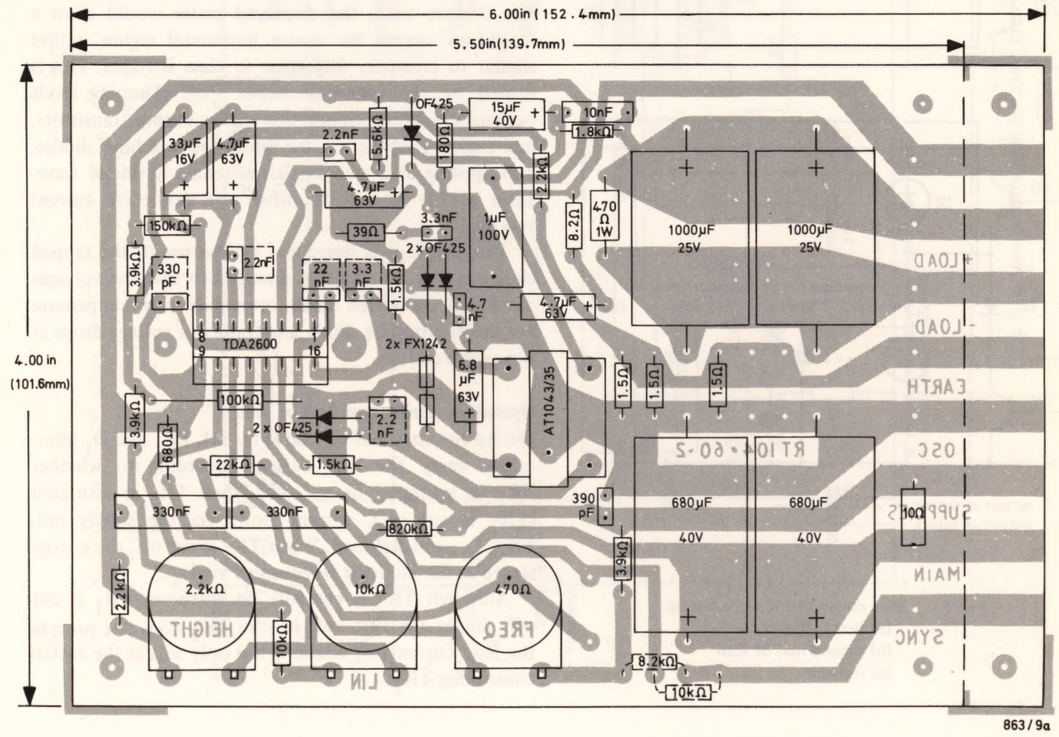


Fig. 9 — Component layout for version of 110° field circuit from component side

2) The 6.8µF supply decoupling capacitor should also be situated near the IC since this capacitor is mainly responsible for keeping the lower frequencies (in the region of medium-wave radio) to a level lower than that produced by other sections of the television receiver. The capacitor should not however be so close as to be heated excessively by the printed-wiring track conducting heat from the IC itself.
3) The energy-recovery diodes OF425 have been chosen since they are fast yet have freedom from the troublesome 'snap action' often associated with fast diodes. It is most important therefore that these diodes are used for optimum results.
4) In all cases of decoupling, the capacitors should be directly connected to the current path itself rather than out on limbs or spurs since the inductor created by a spur can resonate with the capacitor, thus reducing the decoupling.
5) The 1µF filter capacitor should be of a polyester type rather than an electrolytic because of the need for an essentially non-inductive capacitor. The values of ceramic decoupling capacitors should also be kept to the preferred values shown for optimum results.
6) Since the luminance delay line is particularly sensitive to magnetic coupling at the fundamental frequency (150kHz), it is important that this should be at least 15cm away from the filter choke.
7) If complex wiring looms are used where the field connections have long wires closely coupled to other receiver functions, low-level patterning may be displayed.

   If this is so, then a 100nF capacitance placed across the field coil connections on the field board, combined with a small inductor (5µH) in series with the east-west take-off and deflection coil lead connected to the 0.5Ω sensing resistor, may well be found to be a suitable cure.
8) The main decoupling of 2X680µF should be on the field board itself or at least very close to it.
9) It is also recommended that the leads to the capacitor between pins 4 and 9, (330pF) which determines the triangle frequency should be as short as possible, and common impedance paths should be avoided.

Further general points are as follows. Rise-time limiting is carried out in two ways: (a) limitation of the drive waveform dv/dt and (b) limitation of the output waveform dv/dt. Limiting (a) is accomplished by the components 39Ω and 3.3nF connected between pin 3 and earth, and limiting (b) is accomplished by the 3.3nF connected between pin 16 and earth.

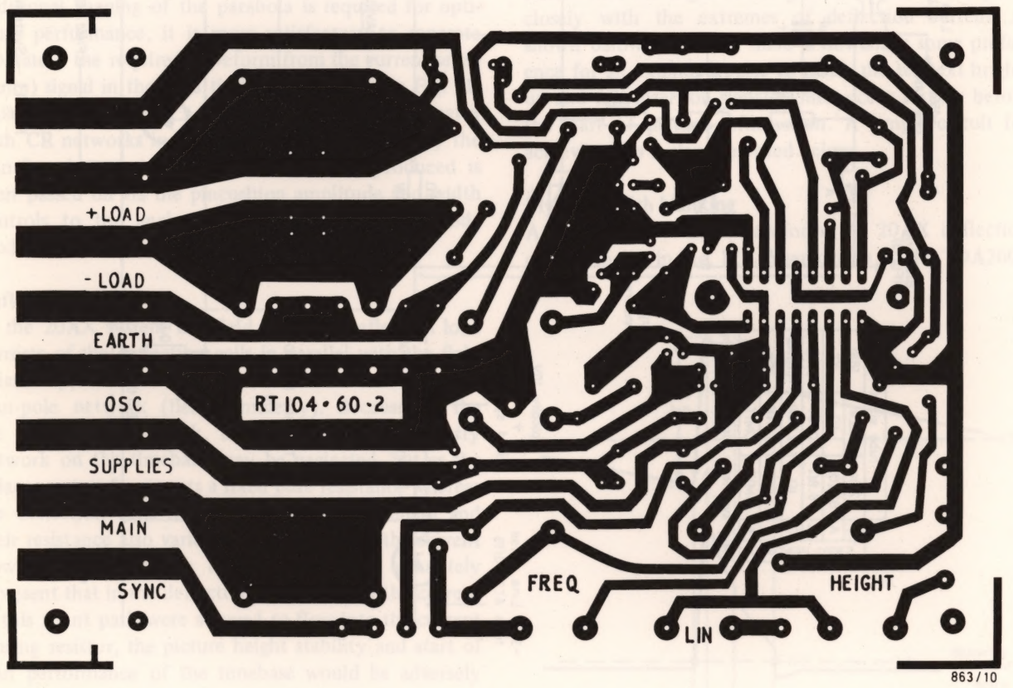


Fig. 10 — Copper side of printed wiring board (actual size)

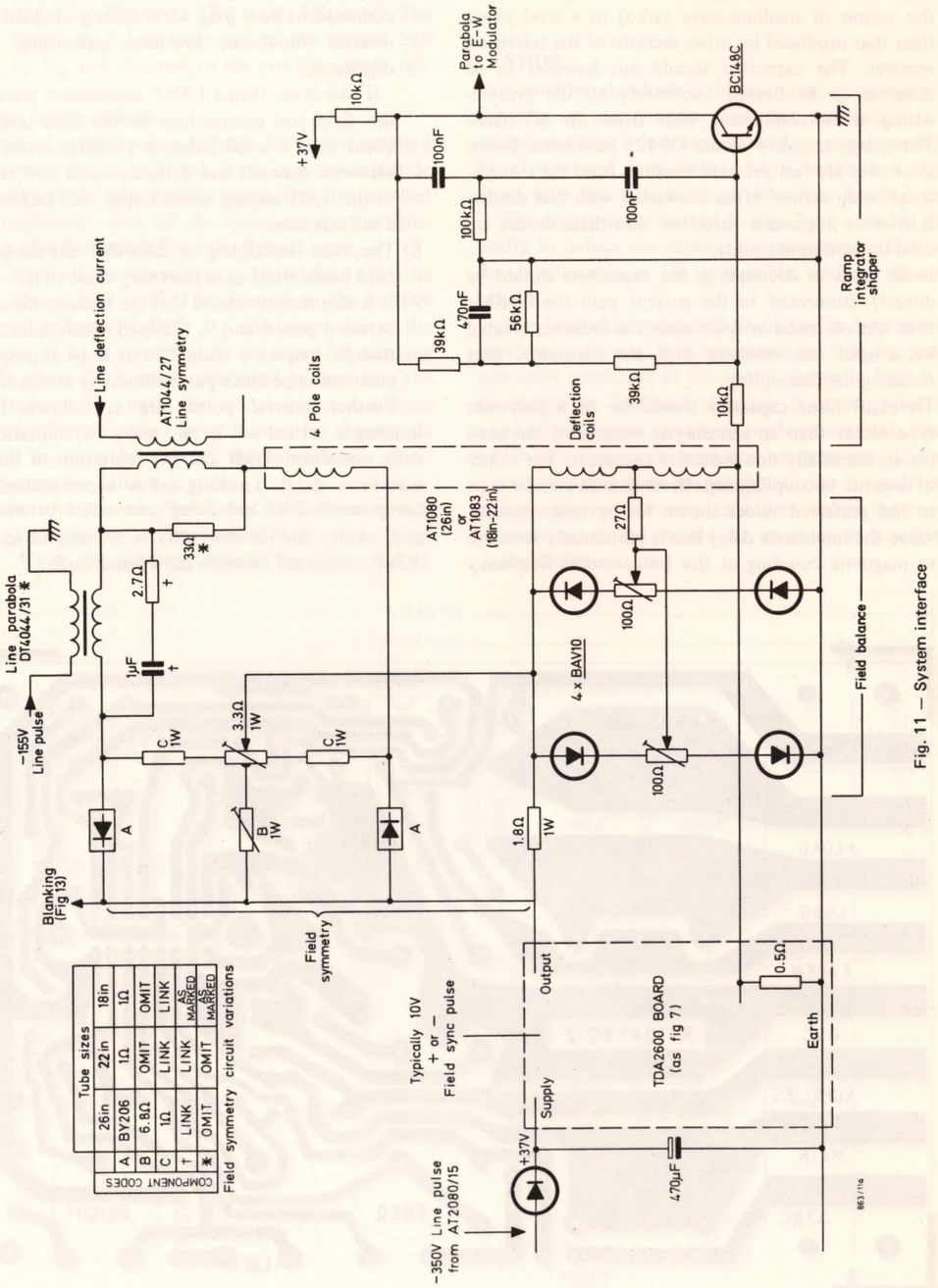


Fig. 11 — System interface

The effectiveness of these measures has been established by measurement of several different receivers, and in all cases no interference problem has been found to exist on Bands I to V with set-top aerials receiving very low level signals.

OVERALL SYSTEM DESIGN FOR 20AX

Fig 11 shows how the field timebase (Fig. 7) interfaces with the other parts of a complete 20AX television receiver. The following sections describe some of the ways that the characteristics of the timebase and its peripheral circuits have affected the design of each other. Heatsink design is described in Appendix 1, and the calculation of supply rail voltages etc. is given in Appendix 2.

East-west modulator

The diode modulator, like any other type of active east-west pincushion correction circuit, requires a low-level parabolic input waveform at field frequency. This is often derived from the parabolic voltage which appears across the field timebase output coupling capacitor. It is necessary, however, to remove ramp and d.c. components, and even then the amplitude of the parabola is subject to variation caused by the temperature coefficient of this electrolytic capacitor. Since the 20AX system requires about 14% east-west correction, and additional shaping of the parabola is required for optimum performance, it is more satisfactory to generate separately the required waveform from the current sense (ramp) signal in the field timebase, as shown in Fig. 11. This stage is basically a simple one-transistor integrator with CR networks in the feedback paths to modify the transfer characteristic. The 'parabola' so produced is then passed on via the pincushion amplitude and width controls to the analogue driver stage and the diode modulator itself, in the normal manner.

Deflection load

In the 20AX system the field timebase deflection load consists of the deflection coils in parallel with the field balance potentiometers, together in series with the four-pole network (field symmetry). Because of the use of current feedback, the effect of the symmetry network on the timebase may be neglected, but as the balance network presents a fixed pure resistance whereas the deflection coils have an inductive component and their resistance also varies with temperature, the current flowing in the balance network does not accurately represent that in the deflection coils. Thus, if the current in this shunt path were allowed to flow into the current sensing resistor, the picture height stability and start of scan performance of the timebase would be adversely affected. For this reason the deflection coils are arranged next to the current sensing resistor, and the field balance path is taken to the remote end of this resistor (earth), as shown in Fig. 11. Therefore, rather unusually for a field timebase, the output coupling capacitor is on the 'high' side of the deflection coils, but this does not have any disadvantages with 20AX because neither an east-west parabola take-off nor a bidirectional picture shift adjustment is required.

The centring accuracy of the 20AX beam is sufficiently high for an adjustable picture shift control to be generally considered unnecessary. However, because of the exponential shape of the flyback current waveform and the presence of undisplayed lines between the nominal end of flyback and the start of picture information, a small consistent upward displacement of the raster is required, and this is provided by the 470Ω resistor which 'bleeds' a current past the output coupling capacitor. If perfect centring of the picture is desired, this resistor can be made adjustable (or selected) to correct for any slight alignment errors of the electron gun.

Blanking

In the past, the vertical blanking signal has usually been derived from the output voltage waveform of the field timebase. This is still possible with 20AX and the TDA2600, provided that precautions are taken to ensure that the edges of the generated pulse correspond closely with the extremes of deflection current, as shown below. However, there is nowadays some preference for an extended pulse to blank the teletext bright-up and test insertion signals which occur shortly before the start of picture information. A simple circuit for achieving this is also presented below.

Flyback width blanking

A typical field drive waveform for 20AX deflection coils is shown in Fig. 12a. When driven by the TDA2600

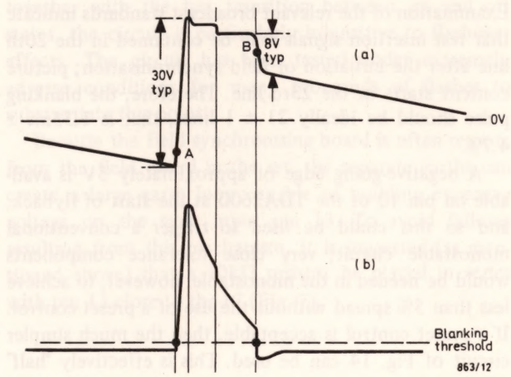


Fig. 12 — Blanking waveforms

circuit, the rising edge of the flyback pulse is not particularly fast because of the presence of the lowpass output filter. It is therefore desirable to initiate the blanking pulse as far down the slope as possible, for example at point 'A'. To allow for spreads, the blanking pulse has to be arranged to terminate near the middle of the falling edge, that is at point 'B'; this is adequate provided that the falling edge is not excessively slow and there are no 'rings' at the start of field scan.

These provisions have been made in the TDA2600 circuit design by optimising the value of the resistor in series with the d.c. feedback decoupling path at 180Ω (Fig.7), and by the connection of the field balance network as already described above.

The points 'A' and 'B' can be easily brought to a single threshold level (one transistor V_{BE}, for example) by using an a.c. coupling with a time-constant of approximately 0.5ms, as shown in Fig. 12b. A complete circuit which incorporates line blanking is shown in Fig. 13. The optional resistor R_X is a refinement to compensate for the negative bias voltage present at the line input between pulses, thereby optimising the blanking threshold.

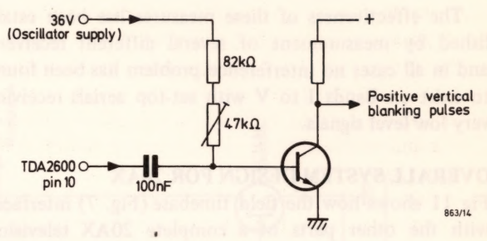


Fig. 14 — Extended blanking circuit

pin 10 varies only in proportion to the ramp generator supply voltage.

Power supply

The ramp generator should be operated from a scan rectified supply to give correct tracking of height with picture width, and it is generally most convenient to use scan rectification for the main timebase supply. The current drawn from the supply rail in any type of field timebase varies considerably during the scanning cycle, and so the timebase is decoupled by a resistor of typically 10Ω as shown in Fig. 7, to prevent the varying load from disturbing the line timebase and affecting the raster shape.

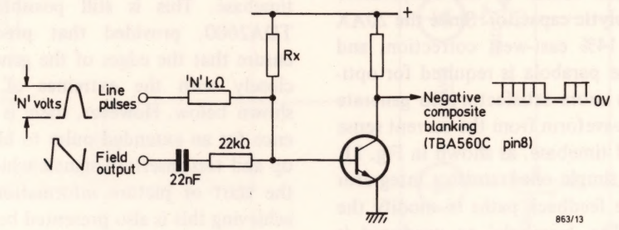


Fig. 13 — Composite blanking circuit

'Extended' blanking

Examination of the relevant broadcast standards indicate that test insertion signals may be contained in the 20th line after the initiation of field synchronisation; picture content starts in the 23rd line. Therefore, the blanking pulse should be ideally 21 ± 1 lines, that is 1.35ms ± 4.7%.

A negative-going edge of approximately 5V is available on pin 10 of the TDA2600 at the start of flyback, and so this could be used to trigger a conventional monostable circuit; very close tolerance components would be needed in the monostable, however, to achieve less than 5% spread without the use of a preset control. If a preset control is acceptable, then the much simpler circuit of Fig. 14 can be used. This is effectively 'half' of a monostable circuit, and uses the characteristic that with any given TDA2600 sample the step amplitude at

It is shown in Appendix 2 that to allow for all spreads, the minimum supply voltage is 36V. This is compatible with the scan rectified voltage from line transformer AT2080/15.

An approximately parabolic ripple voltage of typically 3.5V amplitude appears on the field output stage supply rail with its peak approximately 2V lower than the scan rectified supply voltage. It can be seen from Fig. 4 that to achieve minimum transistor saturation losses, the upper output device needs to be driven from a supply several volts higher than the output stage rail (pin 15). Although this can be obtained with a conventional 'bootstrap' system from the IC switching output (pin 16), a simpler technique is to draw the small

current required by pin 14 from the higher (undecoupled) supply via a 1.5kΩ resistor as shown in Fig. 7. The ripple current in this resistor is comparable to the residual switching ripple through the 10Ω filter resistor, and so any additional filtering required on this rail is minimal.

In a pulse-width modulated system, any variations in the supply voltage produce a proportional change in the system output voltage, and so ripple on the supply rail distorts the output waveform. Current feedback reduces this effect considerably, and the remaining 'error' represents a top-to-bottom non-linearity of 2 or 3% (and also a change in 'S'-correction). As this is a consistent error it may be considered desirable to eliminate it, and this is performed by the 100kΩ resistor from the main supply to the input coupling capacitor (as in Fig. 7). This introduces into the system a signal which compensates the above-mentioned effect.

It was shown above that the output from the ramp generator at the start of scan is a fixed voltage but that the overall amplitude tracks with the oscillator supply rail. Thus the mean level of the ramp changes in unison with the supply, during, for example, variations in beam current. If a sudden large change in beam current occurs, a small instantaneous displacement of the picture is produced: this displacement, however, quickly dies away because of the a.c. couplings in the system. This 'jump' can also be compensated by applying a small fraction of the initiating disturbance on the oscillator supply rail to the inverting pre-amplifier input (pin 6) with a series CR network of typically 390kΩ and 68nF. (In this case, neither the anti-bounce components nor the 100kΩ resistor are used.)

Synchronisation

Synchronisation has already been described above, and the interface is normally straightforward since a suitable pulse is generally available from an IC in the jungle or line oscillator areas. Nevertheless, even if a direct interface between integrated circuits appears satisfactory (between, for example, TDA2590 and TDA2600), it is suggested that a discrete series resistor of about 10kΩ should be included to avoid high circulating currents and possible damage in the event of a picture tube flashover.

Where an interface circuit is required (with, for example, TBA920), it is recommended that this should be incorporated at the signal source because a large-amplitude low-impedance synchronising pulse offers greatest immunity to interfering signals being picked up from other parts of the television receiver.

PERFORMANCE

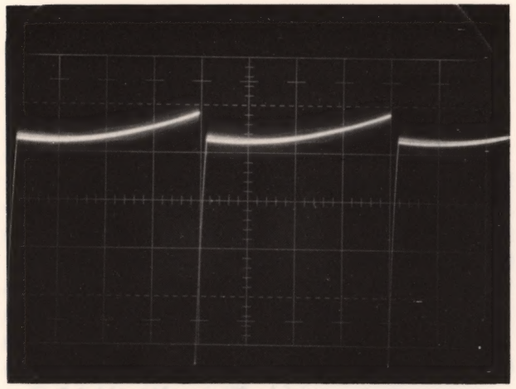
The following measurements have been made with a typical vertical deflection circuit for 20AX (with 25kV e.h.t.) utilising a TDA2600 and series dynamic correction. Various waveforms associated with the circuit are shown in Fig. 15.

Deflection coil type AT1080	
Resistance at 25°C	3.26Ω
Inductance at 25°C	3.48mH
Deflection current (6% overscan)	3.6A
Total load resistance (deflection coil plus series dynamic correction plus sensing resistor)	5.65Ω
Circuit flyback time (typical)	1ms
(absolute maximum)	1.2ms
Input current (typical)	350mA
Supply voltage	36V
IC dissipation (typical)	4.4W
IC dissipation (worst-case and controls maladjusted)	5.6W
Non-linearity of scan	<5%
Switching frequency (typical)	150kHz
Oscillator and ramp generator:	
Frequency variation of field ramp generator over temperature range 20 to 65°C (ambient)	+2%
Field ramp amplitude (synchronised to 50Hz) over temperature range 20 to 65°C (ambient)	+0.5%
Change in field ramp frequency for supply + 10%	+0.5%

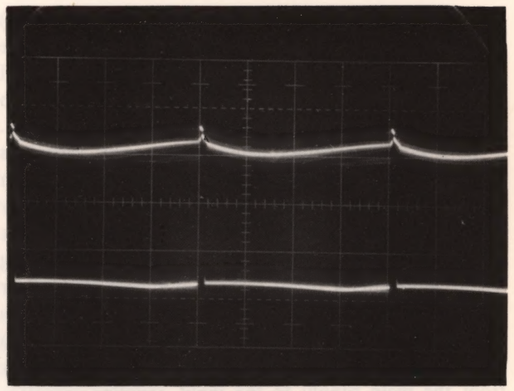
FLASHOVER

Flashover of the e.h.t. picture tube can lead to failures of conventional circuitry, particularly in the field section, because of the coupling between the field and line deflection coils and the tube aquadag. With the TDA2600, because of the isolation of the filter choke, the 1μF filter capacitor, and the energy-recovery diodes, together with the fast transition between on and off states, the circuit is particularly insensitive to flashover effects. The circuit has been tested under extremely adverse conditions for many thousands of flashes to substantiate this point.

Because the field synchronising board is often remote from the field board in the set, the separate earths can create a large earth loop capable of building excessive voltage on the sync input pin 13. To avoid failures resulting from this mechanism, it is suggested (as mentioned above) that a 10kΩ resistor be placed in series with pin 13 close to the IC (Fig. 7).



(a)



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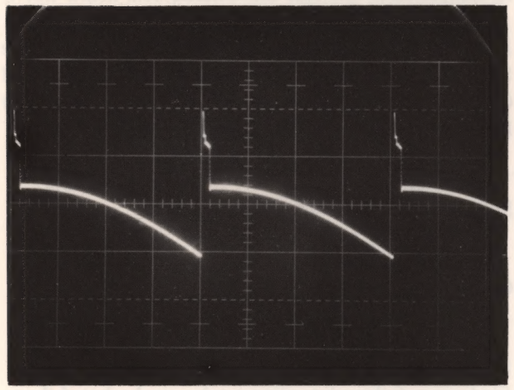

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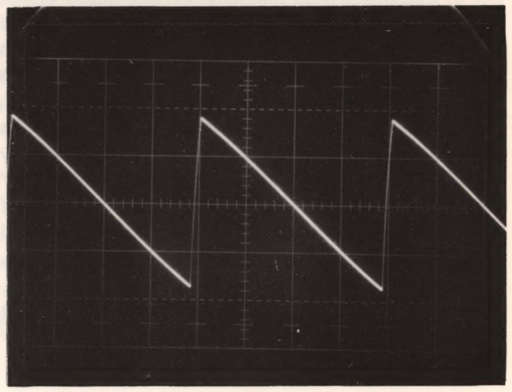

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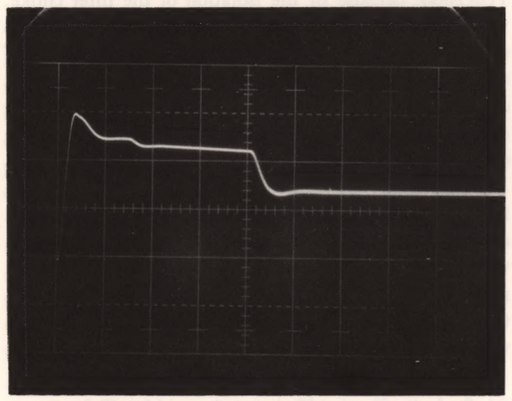

(e)

Fig. 15 — Oscilloscope displays of waveforms as follows:
(a) pre-amplifier input signal at pin 7 (200mV and 5ms per main division)
(b) switching envelope waveform at pin 16 (10V and 5ms per main division)
(c) field output from AT4043/35 filter choke (10V and 5ms per main division)
(d) deflection coil current measured across 0.5Ω sensing resistor (500mV and 5ms per main division)
(e) field flyback waveform at the output of the AT4043/35 filter choke (10V and 200μs per main division)

APPENDIX 1
Heatsink Design

The TDA2600 has a measured junction-to-heatsink thermal resistance of typically 3.2degC/W in practice. For the following calculations a figure of 4degC/W has been allowed.

The IC junction temperature is calculated on an 'average working temperature over life' basis since this is the factor that determines m.t.b.f. The average working temperature over a working life of 30 000h has been taken as 100°C since no significant change in m.t.b.f. will occur below 110°C. The nominal dissipation of the IC for 20AX applications is 4.4W, thus a 17.6degC rise above the heatsink temperature is obtained for T_j.

Assuming a nominal set temperature of 45°C, this gives a total of 62.6°C for T_j with an infinite heatsink.

Therefore, for T_j = 100°C the heatsink thermal resistance is (100 – 62.6)/4.4degC/W, or approximately 8.5degC/W.

Measurements of the absolute maximum dissipation of the IC under worst-case conditions will not exceed 5.6W, thus giving a worst-case T_j of 115°C at 45°C receiver ambient.

At 60°C receiver temperature with worst-case conditions, the T_j is thus 130°C.

APPENDIX 2
Supply Voltages

The method of calculating the correct supply and mean output voltages for the 20AX tube system utilising the AT1080 is described below. The AT1080 deflection coil specification is given below.

$I_{pk\text{-}pk}$ for 6% overscan	=	3.6A
R_{yoke} at 25°C	=	3.26Ω
at 75°C	=	3.9Ω
L_{yoke}	=	3.48mH

Definition of terms

The following list gives various terms which relate particularly to the waveform given in Fig. 16.

$+E_{pk}$ is the voltage from the mid-point to the flyback clamping voltage, which is necessary to achieve the required 1.2ms worst-case flyback time.

$-E_{pk}$ is the negative sawtooth component required to produce the end-of-scan current (including 6% overscan).

V_{av} is the required average output voltage above earth including all circuit drops, such as transistor saturation, etc.

V_{top} is the required margin between the average output voltage and the supply voltage during flyback.

$$I_m = \frac{I_{pk\text{-}pk}}{2}$$

τ = deflection coil time-constant

$$= \frac{\text{total load inductance}}{\text{total load resistance}}.$$

t_f is the flyback time, taken as 1.2ms worst-case.

T = scan time = 18.8ms.

V_{cp} = mean-to-peak value of the coupling capacitor ripple voltage.

Additional circuit parameters are as follows: the value of $R_{sensing}$ is 0.5Ω, and the series dynamic correction resistance is 1.25Ω; therefore the total resistive load R_L is 5.65Ω at 75°C. The value of L_1 is 0.15mH, and so L_L (total load inductance) is 3.63mH. The value of τ is equal to L_L/R_L, that is 0.64.

The value $+E_{pk}$ may now be calculated from the following equation:

$$+E_{pk} = I_m R_L \frac{1 + e^{(-t_f/\tau)}}{1 - e^{(-t_f/\tau)}}$$

Therefore:

$$+E_{pk} = 13.8V;$$

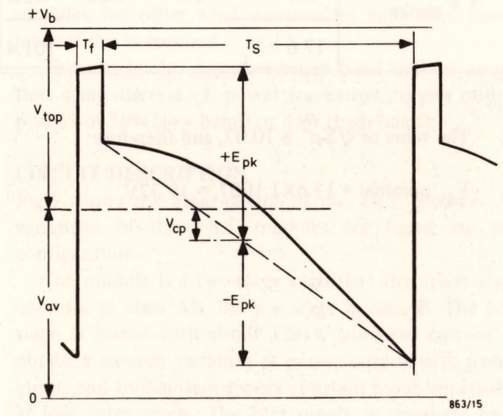

Fig. 16 — Definitions of parameters used in spread analysis. Note that V_{cp} = ⅔ x peak-to-peak parabola voltage across the 2000μF coupling capacitor

and:

$$-E_{pk} = I_m R_L + \frac{L_L . I_M.^2}{T}$$

$$= 10.2 + 0.7,$$

$$= 10.9V.$$

A spread of 8% should be allowed on these figures for e.h.t. and coil sensitivity spreads.

The value of V_{cp} for the output coupling capacitor ($2 \times 1000\mu F$) is 3V, and the tolerance on this capacitor −10% gives a spread of 0.3V. The average output voltage can spread because of IC parameters and component tolerances, and a comprehensive figure for the average output voltage spread ΔV_s is ± 1V.

Calculation of Average Output Voltage V_{av}

The value of V_{av}, the average output voltage, can be calculated by using the values given below.

Variable	Nominal value	Spread V	ρ = % of V_r	ρ^2
$-E_{pk}$	10.9	0.9	5.0	26.0
$\Delta R_y \pm 7\%$	–	0.5	2.8	7.9
V_{cp}	3.0	0.3	1.7	2.9
ΔV_s	–	1.0	5.68	32.3
$V_{ce\ sat} + V_{diode} + V_{choke}$	3.7	1.0	5.68	32.3
	$17.6 = V_r$			101.4

The value of $\sqrt{\Sigma\rho^2}$ is 10.07, and therefore:

V_{av} nominal = 17.6×1.1007, = 19.37V.

Margin between V_{av} and supply voltage during flyback (V_{top})

For the calculation of margin between V_{av} and supply voltage during flyback, the +50% spread on the 2000μF coupling capacitor must be taken into account giving a spread of 1V. The figure required can then be calculated from the ensuing tabulated values.

Variable	Nominal value	Spread V	ρ = % of V_T	ρ^2
$+E_{pk}$	13.8	1.1	8.5	72.0
$\Delta R_y \pm 7\%$	–	0.25	1.95	3.8
V_{cp}	-3.0	1.00	7.80	61.0
ΔV_s		1.0	7.80	61.0
$V_{ce\ sat} + V_{choke}$	2.0	0.5	3.80	14.5
Δ V ripple	–	1.2	9.30	86.0
	$12.8 = V_T$			278.3

The value of $\sqrt{\Sigma\rho^2}$ is 17.27, and therefore:

$$V_{top} = 12.8 \times 1.1727,$$

$$= 15V.$$

The minimum supply voltage requirement under worst-case conditions is the sum of $(V_{av} + V_{top})$ = (19.37 + 15) = 34.37V. This voltage represents the peak of the parabola on the supply rail (pin 15); a figure of 35V has been taken as the design figure. The mean supply voltage on pin 15 will therefore be 32.5V and, allowing for the 10Ω supply decoupling resistor, the input voltage to the unit will be 10Ω×0.35A (mean input current), or 3.5V higher.

The total input voltage requirement is thus (32.5 + 3.5)V = 36V.

Transmitter design with v.h.f. broadband amplifier modules

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This article describes four v.h.f. broadband power amplifier modules and gives related performance and application information. The modules BGY32 and BGY33 cover the band 68MHz to 108MHz, and give 18W output for 100mW drive; the modules BGY35 and BGY36 cover the band 132MHz to 174MHz, and give 18W output for 150mW drive. (These devices are the production modules derived from the development types 438BGY and 437BGY and their variants.)

INTRODUCTION

Mullard v.h.f. power amplifier modules have been introduced to simplify the design and construction of radio transmitters. The modules are intended mainly for use in f.m. mobile radio equipment where space considerations are invariably a high priority.

Techniques are used in the construction of power modules which would be impossible using discrete components. The passive components of the circuit are mounted in close proximity to the active transistor chips, and interconnections are made by semiconductor wire bonding techniques, giving consistent performance from module to module and reducing to a minimum the stray reactances normally present in discrete encapsulations. Very small components can be used: for example, it is possible to fabricate accurately inductances from 1 to 10nH, and to use chip or MOS capacitors with very low self-inductance.

Construction methods such as the above have resulted in the production of a wideband high-power amplifier, of consistent precisely-defined performance, occupying a small space. User adjustments are not provided, because they are unnecessary. The current range of v.h.f. modules consists of the following four types:

BGY32	68 to 88MHz,
BGY33	80 to 108MHz,
BGY35	132 to 156MHz,
BGY36	148 to 174MHz.

All of the devices give a minimum of 18W output when fully driven, the drive power for the lower frequency pair being 100mW and that for the upper frequency pair being 150mW. The manufacturing techniques for these modules enable the construction of modules for other v.h.f. frequencies and other power levels if this is required.

This article also describes broad band 'add-on' amplifiers using discrete r.f. power transistors, to give output powers of 50W (low band) or 45W (high band).

CIRCUIT DESCRIPTION

Fig.1 shows the basic circuit of the v.h.f. module. All variations of the v.h.f. modules are based on this configuration.

The module is a two-stage amplifier: the driver stage operates in class AB, the p.a. stage in class B. The first stage is biased with about 12mA quiescent current to obtain a smooth variation of power output with power input, and to maintain a more constant input impedance at low drive levels. The bias supply is stabilised by a transistor chip whose characteristics closely match those of the driver transistor. This system ensures a constant biasing point over the operating temperature range of the module.

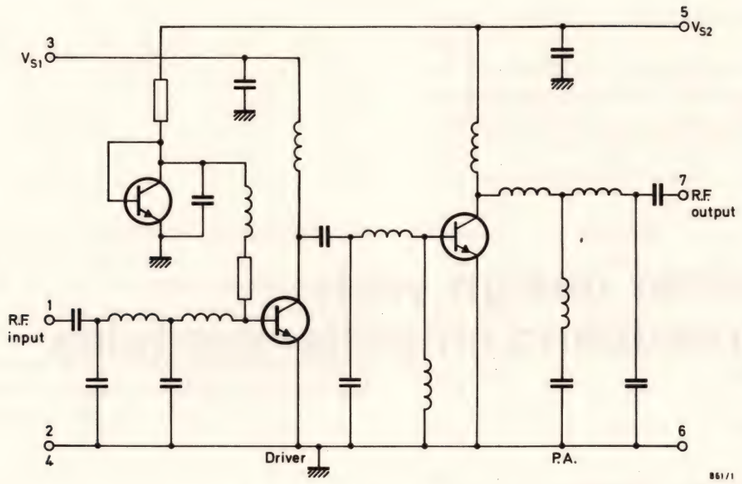


Fig.1 — Circuit of the v.h.f. module

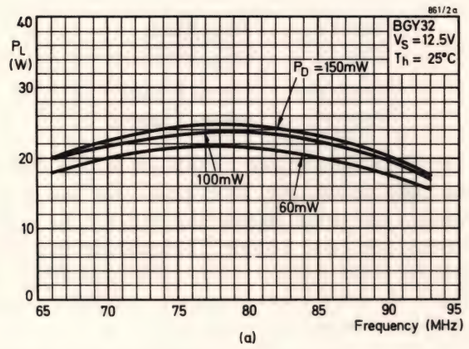


Fig.2 — Typical load power plotted against operating frequency:
(a) BGY32 (b) BGY36

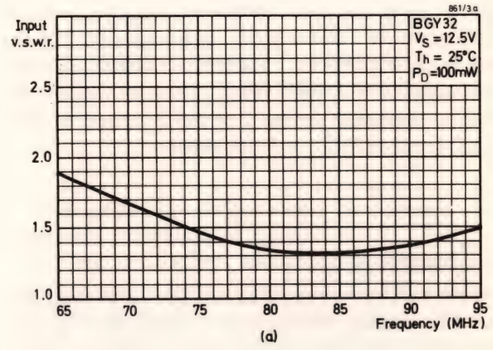


Fig.3 — Typical input v.s.w.r. plotted against operating frequency:
(a) BGY32 (b) BGY36

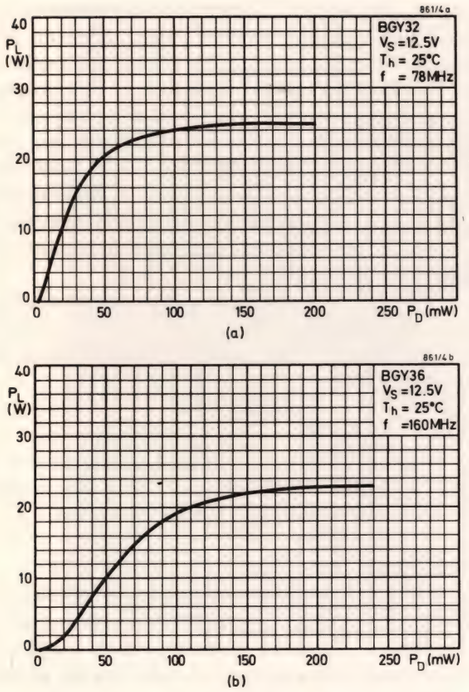


Fig.4 — Typical load power plotted against drive power, at a constant mid-band frequency:
(a) BGY32 (b) BGY36

The input coupling network is a two-stage Chebychev lowpass impedance-transforming network. A similar network, incorporating a second-harmonic trap to improve the harmonic rejection, is used at the output. Interstage coupling is by means of a combination lowpass/highpass network: this configuration makes maximum effective use of a minimum of components.

The h.t. supply voltages to the driver stage (V_{s1}) and the p.a. stage (V_{s2}) are brought to separate pins. Because of this, it is possible to control the power output from the module by varying the driver stage supply voltage.

PERFORMANCE

The specifications of the modules are given in Table 1. Typical performance curves for the low-band BGY32 and high-band BGY36 modules are given in Figs.2 to 4. Fig.2 shows the variation in output power with frequency; Fig.3 shows the variation in input v.s.w.r. with frequency; Fig.4 shows the variation in output power with input power, at a constant frequency (mid-band). The curves are plotted for a heatsink temperature of 25°C.

The guaranteed maximum harmonic content of the output is −25dB, but in practice the harmonic output is usually considerably less than this. Depending upon frequency, values between −35 and −50dB are typical for all the modules.

TABLE 1

Module Specifications

Type number Development number		BGY32 438BGY	BGY33 438BGY/H	BGY35 437BGY/L	BGY36 437BGY/A	
Mode of operation		f.m.	f.m.	f.m.	f.m.	
Frequency range		68 to 88	80 to 108	132 to 156	148 to 174	MHz
Drive power	nom.	100	100	150	150	mW
Output power	min.	18	18	18	18	W
	typ.	23	22	22	21	W
Supply voltages V_{s1} and V_{s2}	nom.	12.5	12.5	12.5	12.5	V
Input impedance	nom.	50	50	50	50	Ω
Output load impedance	nom.	50	50	50	50	Ω
Heatsink temperature (operating)	max.	90	90	90	90	°C
Input v.s.w.r.	typ.	1.5:1	1.5:1	1.5:1	1.5:1	
Harmonic output	max.	−25	−25	−25	−25	dB

MOUNTING

The following guidelines should be followed to ensure optimum performance and reliability from these v.h.f. modules.

Heatsink

The module should be mounted on a heatsink of adequate size. At full power the module normally dissipates 20 to 25W, but with a severely mismatched load the dissipation can rise to 50W or more.

The heatsink should be flat, and the mounting holes free from burrs or thickening. To improve thermal contact, a thin layer of void-filling compound should be used between the module mounting base and the heatsink.

Connections

To obtain maximum output power, it is important to present the module with a load impedance of 50Ω (see section 'Mismatched loads' later). With a conventional power amplifier using discrete components, the output matching network can normally be peaked to match any of a range of load impedances, and the effects of badly-matched filters and cables can be largely 'tuned out'. Modules, however, are constructed in a precise and well-defined manner, and the output terminal requires a precise 50Ω load. It is therefore necessary to use correctly-matched filters, with 50Ω cable for interconnections. The module leadouts should be trimmed to about 2mm.

Flat strips, 0.1mm thick, are used for the module leadouts: they are particularly suitable for printed-wiring board connection. Input and output lines of 50Ω characteristic impedance can be fabricated directly on the printed-wiring board. Examples of this stripline technique can be seen in Fig.5, which shows part of a complete transmitter chain to be described later. The printed-wiring board must be of low-loss material, such as epoxy glass-fibre, with bare copper on the underside to act as a ground plane. For a characteristic impedance of 50Ω on a 1.5mm (1/16in) epoxy glass-fibre board, the width of the line is approximately 2.5mm.

Coaxial cable can also be used for the input and output lines, as shown in Fig.6. Care should be taken to make the transition from cable to module as physically small as possible.

SUPPLY VOLTAGE

The modules are primarily designed for application in mobile communications equipment where they operate from the 12V (nominal) vehicle electrical system.

Supply voltage decoupling

Decoupling components are included in the modules, but the additional decoupling arrangement shown in Fig.7 is recommended. The extra capacitors ensure stability at low drive levels with a mismatched load; they also prevent the generation of wideband noise under certain mismatched conditions, and help to suppress power supply instability when modules are operated from certain types of electronically-stabilised power supplies.

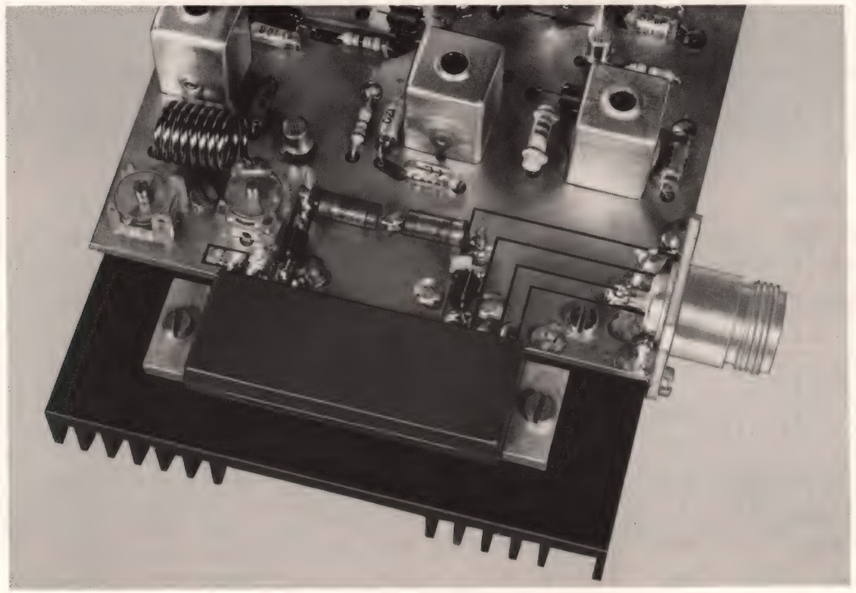


Fig. 5 – Part of a complete transmitter chain using the BGY32 showing fabricated stripline interconnections

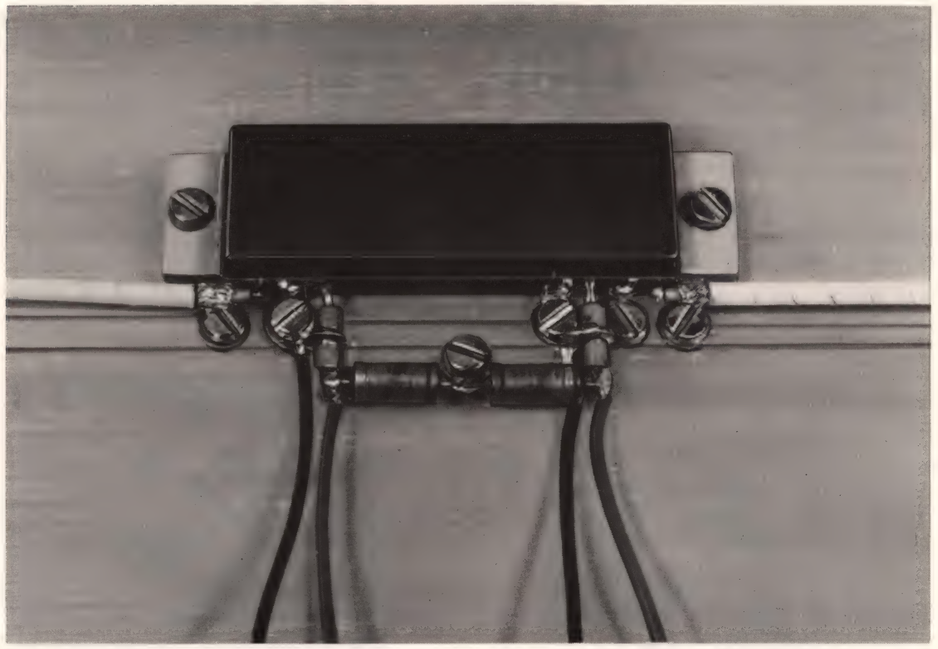


Fig.6 – Module with coaxial cable input and output lines.

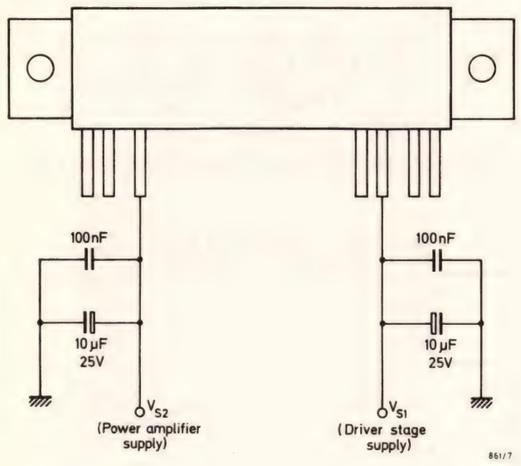


Fig.7 – Recommended decoupling arrangement

Operation from supplies other than 12V

The maximum rated supply voltage (V_{s1} and V_{s2}) for all the modules is 15V, and so the modules can operate from 12V vehicle electrical systems. If it is required to operate the module from a supply rail at a higher voltage, then a voltage-limiting circuit must be used. Two possible circuits are shown in Fig.8. Circuit (a), with a 3A current rating, or circuit (b), rated at 5A, should be chosen according to the power consumed by the module in the particular application. The current rating of circuit (a) may be increased to 4A by using a BD434 transistor for TR_1 and reducing resistor R_3 to 120Ω. In addition to the current drawn by the module, the 3A circuit draws a further 0.1A from the supply, and the 5A circuit a further 0.5A.

The limited output voltage is determined by the voltage regulator diodes D_1 and D_2, and can be altered by replacing these components according to the equation:

$$V_{limit} = V_z + 0.7,$$

where V_{limit} is the limited output voltage and V_z is the

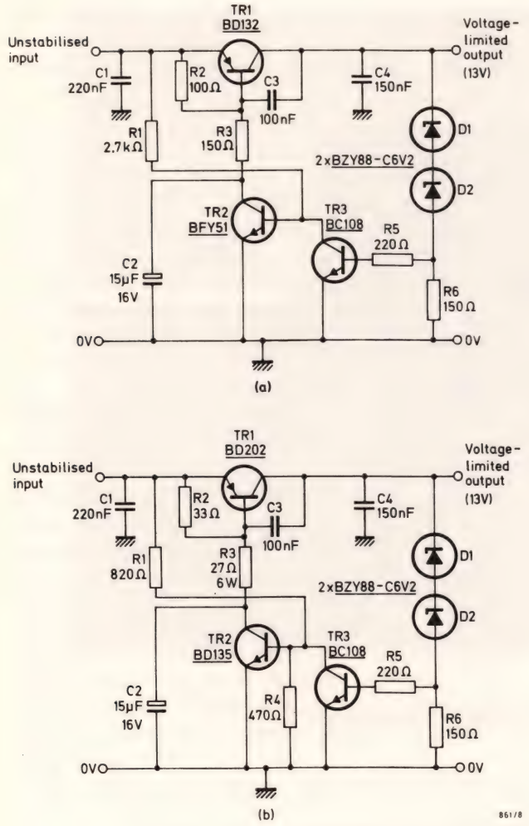


Fig.8 – Voltage-limiting circuits:
(a) 3A rating; (b) 5A rating

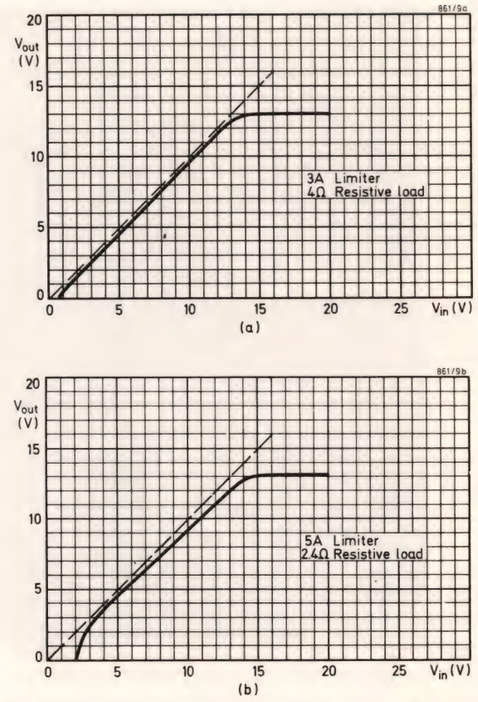


Fig.9 – Voltage limiter performance: (a) 3A circuit; (b) 5A circuit

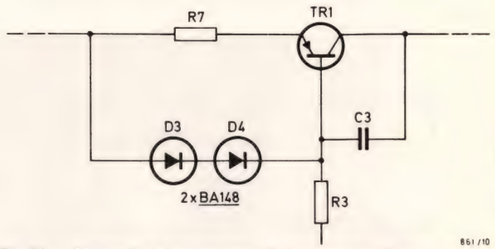


Fig.10 – Alternative arrangement to give current-limited output

total breakdown voltage of D_1 and D_2. Performance curves for the two circuits are given in Fig.9.

The facility of current limiting may be added to either of the circuits of Fig.8 by deleting resistor R_2 and adding components R_7, D_3, and D_4, shown in Fig.10. Current limiting reduces module dissipation, and hence the required heatsink size, under severe load mismatch conditions. However, it increases the voltage drop across the voltage limiter by up to 0.8V, marginally reducing the r.f. power output available from the module under normal conditions.

For the circuit of Fig.10 the limited output current I_{limit} is determined by the value of resistor R_7 in series with the emitter of the control transistor TR_1. Approximate values of R_7 for various current limit levels are given in Table 2.

TABLE 2 Selection of Resistor R_7

I_{limit} (A)	R_7 (Ω)
1	0.70
2	0.35
3	0.23
4	0.18
5	0.14

OUTPUT CONTROL

The modules are designed to give full output power (>18W) when operating from a 12.5V supply with a drive power of 100mW for the low-band modules or 150mW for the high-band modules. To obtain lower levels of output power, either the drive power or the supply voltage may be reduced.

The effects of reducing the drive power have already been shown, in Figs.2 and 4. The effects of reducing the module supply voltage are shown in Fig.11 for the BGY32, and in Fig.12 for the BGY36. Both the driver (V_{s1}) and p.a. (V_{s2}) supply voltages may be reduced together, or else V_{s1} may be reduced while V_{s2} remains constant.

The relative advantages and disadvantages of each method of output control are now discussed.

R.F. drive control

This system requires no additional h.t. control circuitry, and can yield the highest overall efficiency. However, at low power it is difficult to maintain a stable level of output power because of the steep control characteristic:

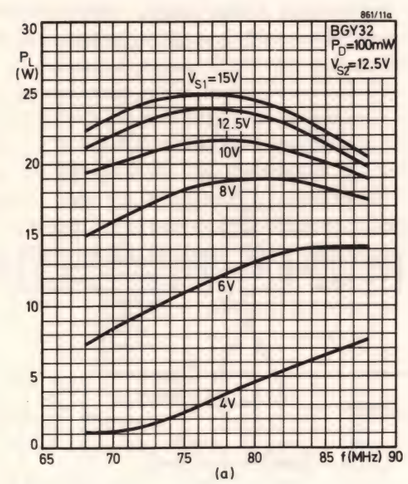


Fig.11 – Typical load power plotted against operating frequency (BGY32):
(a) with variable V_{s1}; (b) with variable V_{s1} and V_{s2}

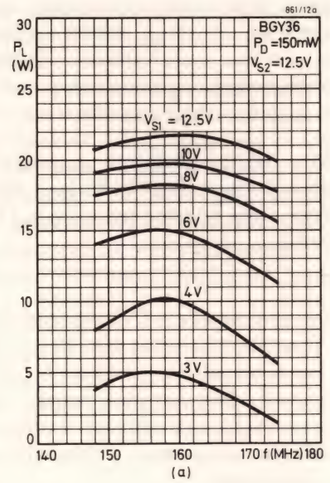


Fig.12 – Typical load power plotted against operating frequency (BGY36):
(a) with variable V_{s1}; (b) with variable V_{s1} and V_{s2}

see Fig.4. Variations in drive power, due to the effects of changes in temperature, voltage, and frequency on preceding driver and multiplier stages, will strongly affect the output power and may require some form of r.f. feedback control. There may also be a considerable spread of output power at low drive level between individual modules.

V_s control

It can be seen from Figs.11 and 12 that reducing the output power by reducing both V_{s1} and V_{s2} gives a more constant output power over the frequency range than is achieved by reducing V_{s1} only. Reducing both V_{s1} and V_{s2} also gives a higher module efficiency, but if the dissipation in the supply voltage control circuit is taken into account then the overall efficiency is similar. A high-power voltage-regulating circuit, capable of delivering a current up to 5A, is necessary: the circuit of Fig.8b is suitable.

The stability of the module is guaranteed for a minimum supply voltage of 10.5V. To keep within this recommendation, only a limited reduction in r.f. power output is possible.

V_{s1} control

For best overall performance, it is recommended that the r.f. output power be controlled by varying V_{s1}, the driver stage supply voltage. Variations in r.f. drive power then have minimal effect on power output, and high-power/low-power switching is easily accomplished. However, the variation in power output is higher at low values of V_{s1} than at full power.

A supply voltage regulator, to supply a current up to 0.6A at between 3 and 12V, is required. A suitable circuit is shown in Fig.13, and in the two complete circuits described later.

The modules have been optimised for use at the full output power level. At reduced power, some sacrifice in efficiency is unavoidable. Efficiency in the region of 45 to 55% is achieved at full output; reducing V_{s1} to obtain 8W output will give 30 to 35% efficiency.

Two possible feedback power control systems are shown in Fig.14. (These are for use with the control amplifier shown in Fig.13.) System (a) in Fig.14 restricts the r.f. power output when operating with a mismatched load, to improve the module reliability and reduce the dissipation. System (b) allows operation at reduced power, and gives a flatter output power/frequency characteristic than could be achieved with simple fixed voltage control.

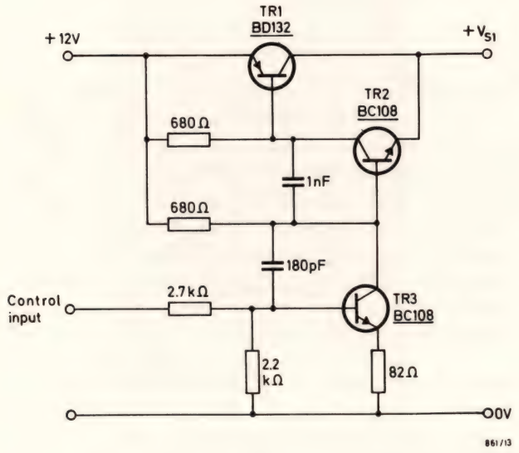


Fig.13 — Supply voltage control amplifier

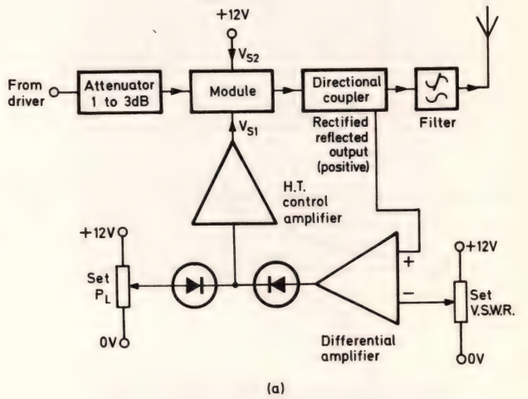


Fig.14 — Feedback control systems:
(a) to limit power output into mismatched load;
(b) to limit power output and give flat power-frequency relationship at low power

DRIVE UNITS

Frequency generation, modulation, and drive unit design for a complete transmitter using a v.h.f. module can follow conventional practice. It is essential, however, that the drive signal to the module is 'clean', having low spurious-signal content. The module makes use of low-pass networks, and any spurious signals present on the drive signal, within the module passband or at lower frequencies, will be amplified and fed to the aerial.

If a conventional crystal oscillator-multiplier chain is used for driving the module, then sufficient rejection of unwanted signals can normally be achieved with double-tuned circuits between stages. For maximum rejection the tuned circuits should have a high loaded Q. An alternative system, giving an output which is inherently clear of unwanted signals, drives the module from an oscillator operating on the final carrier frequency which is phase-locked to a multiple of a reference crystal oscillator. This system represents a considerable saving in tuned circuits and can be broadband in operation. Together with the broadband characteristics of the v.h.f. modules, this system enables wideband transmitters to be more readily designed. Block diagrams of both systems are given in Fig.15.

Complete circuits

The circuits of complete transmitters using the BGY32 and BGY36 are given in Figs.16 and 17. Conventional circuit techniques are used. Both designs are capable of low spurious output: better than −65dB relative to the carrier frequency, with the exception of the second and third harmonics which can be suppressed by a lowpass filter at the module output.

In Figs.16 and 17, a crystal oscillator is followed by a phase modulator and a ×12 multiplier chain. Multiplication is achieved in three stages: ×3, ×2, ×2. Double-tuned circuits are included between stages. The multiplication of ×12 is adequate to achieve 7kHz deviation at the final frequency. The r.f. output power of the final doubler is 130mW for the 84MHz transmitter and 180mW for the 168MHz transmitter.

A suitable printed-wiring board design is given in Fig.18, and the component layout in Fig.19. No attempt at miniaturisation has been made in this design; a much more compact layout would be required and achievable in practical mobile equipment. Fig.20 is a photograph of the board together with the module mounted on a heat-sink. A components list with coil-winding details appears in Appendix 1. The board is of 1.5mm (1/16in) double-

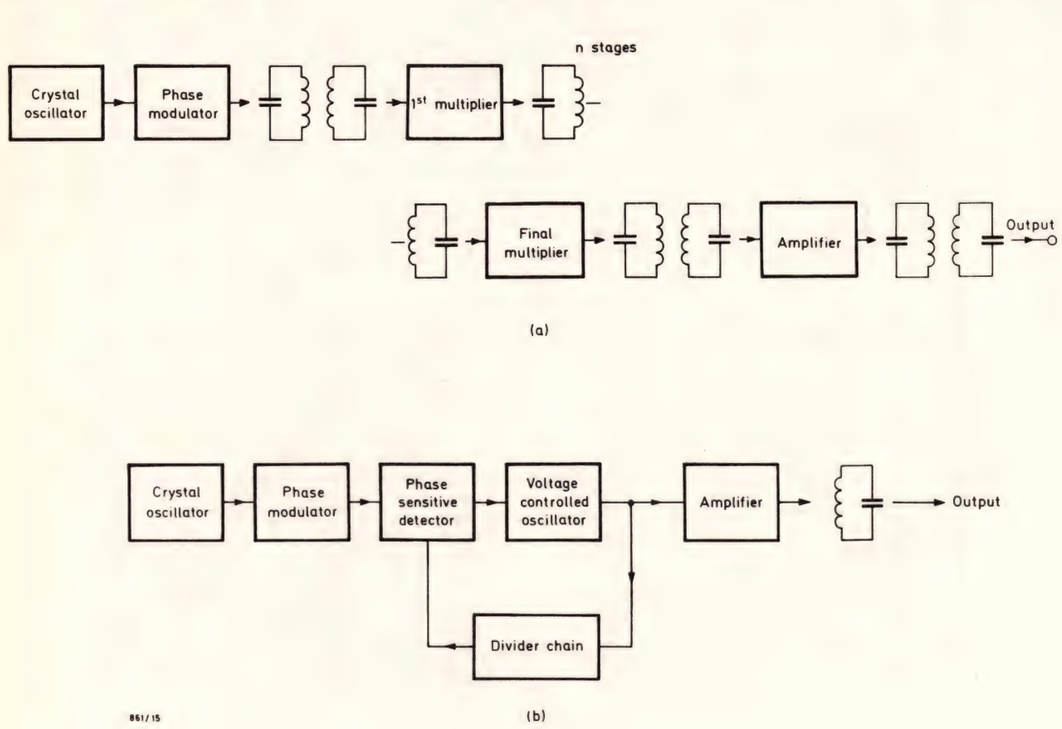


Fig.15 — Transmitter drive systems:
(a) crystal oscillator-multiplier; (b) phase-locked divider

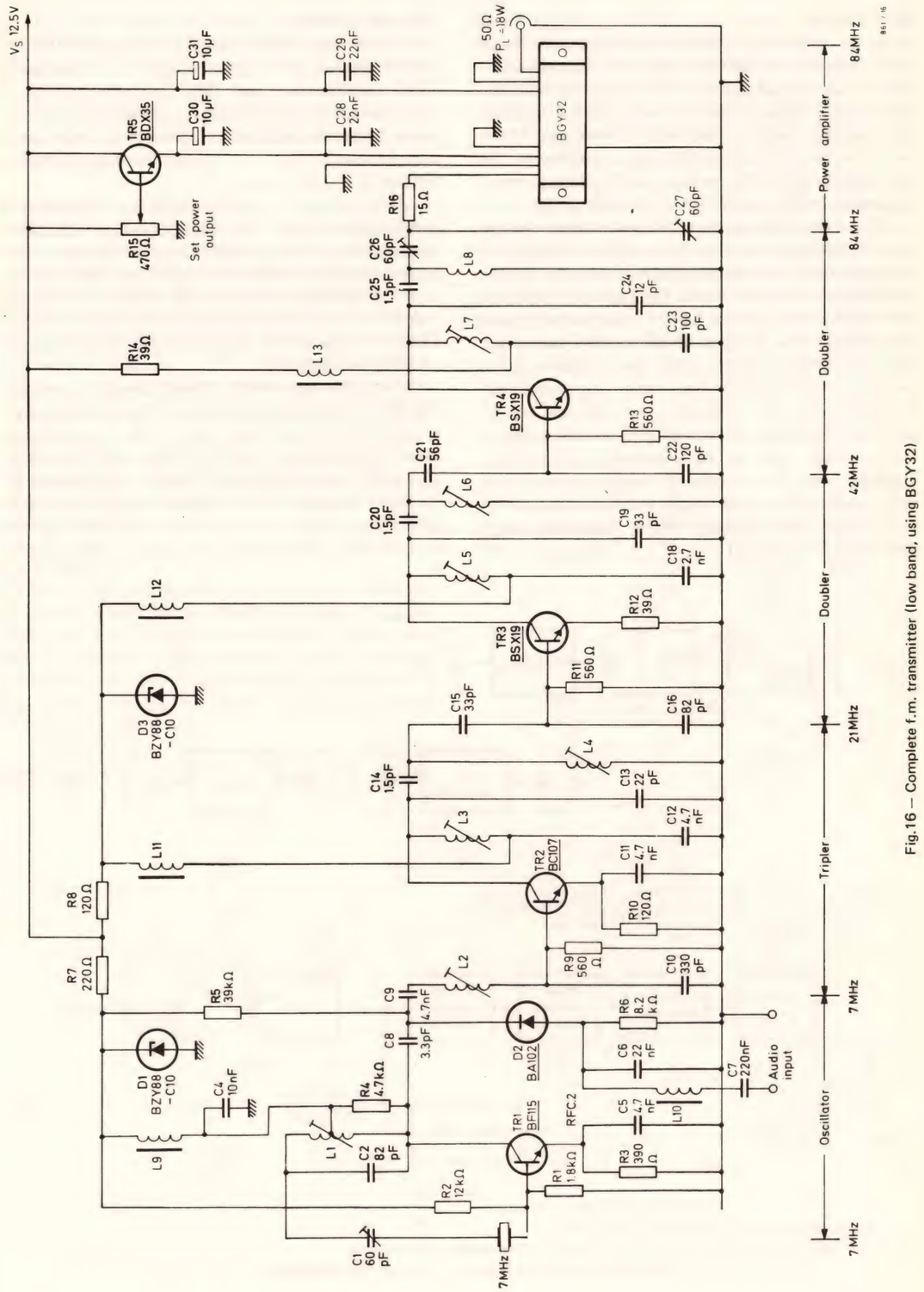


Fig.16 — Complete f.m. transmitter (low band, using BGY32)

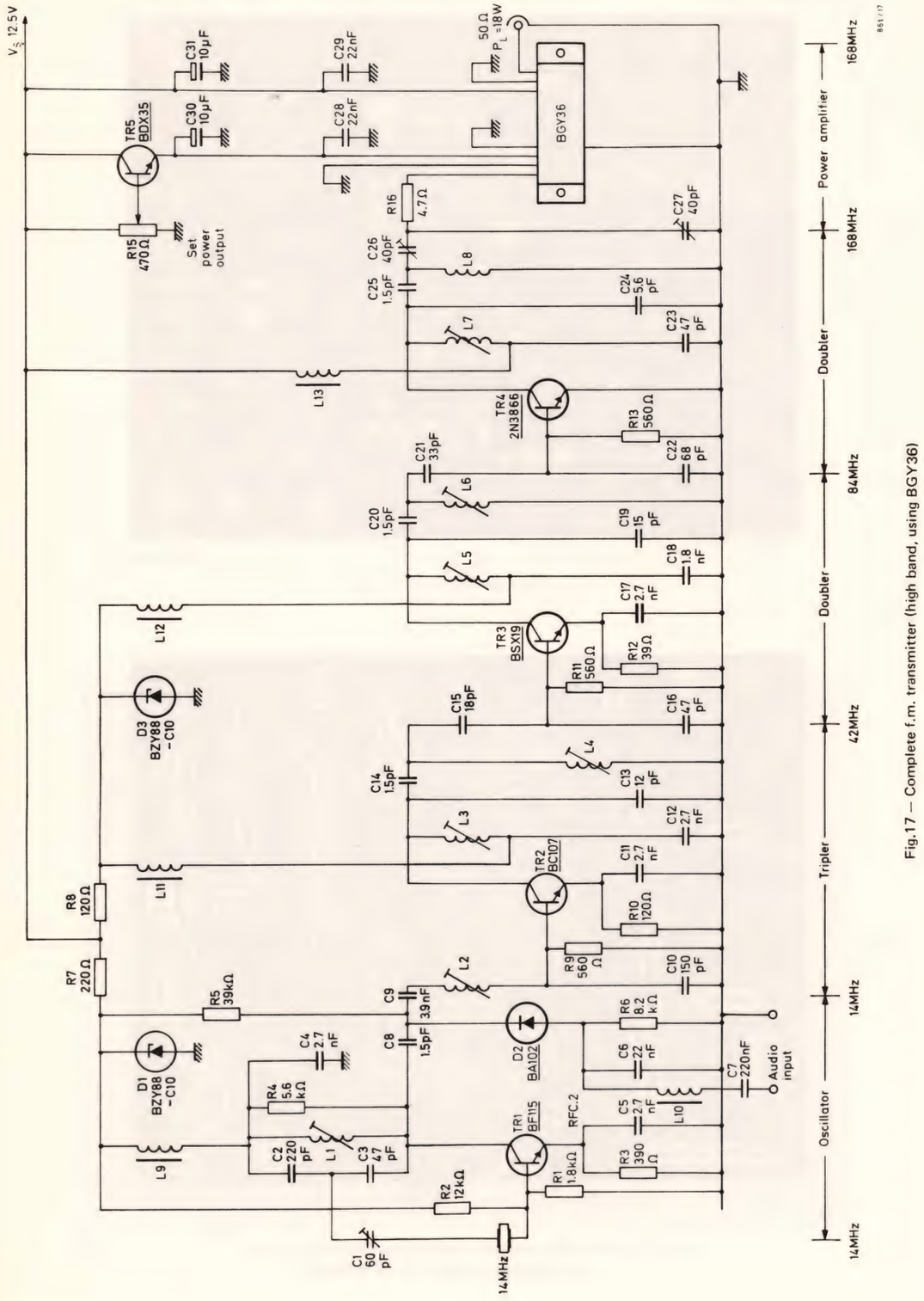
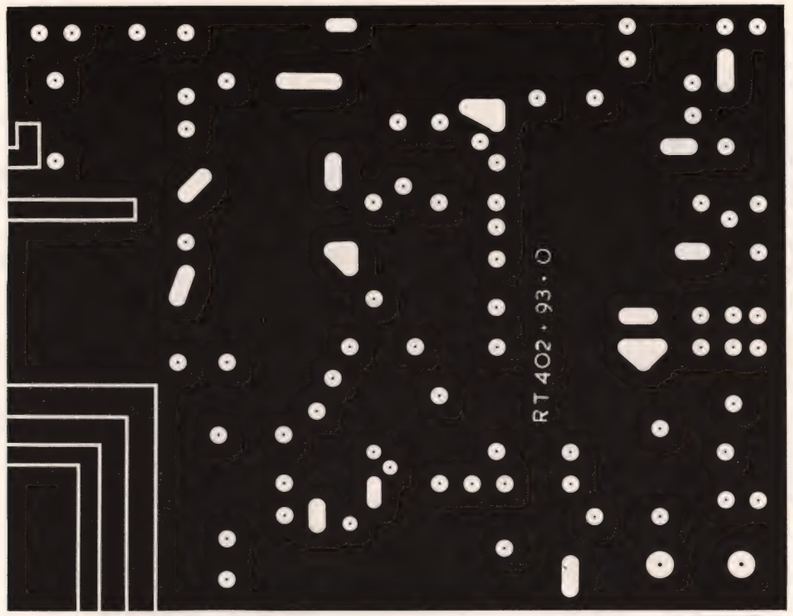
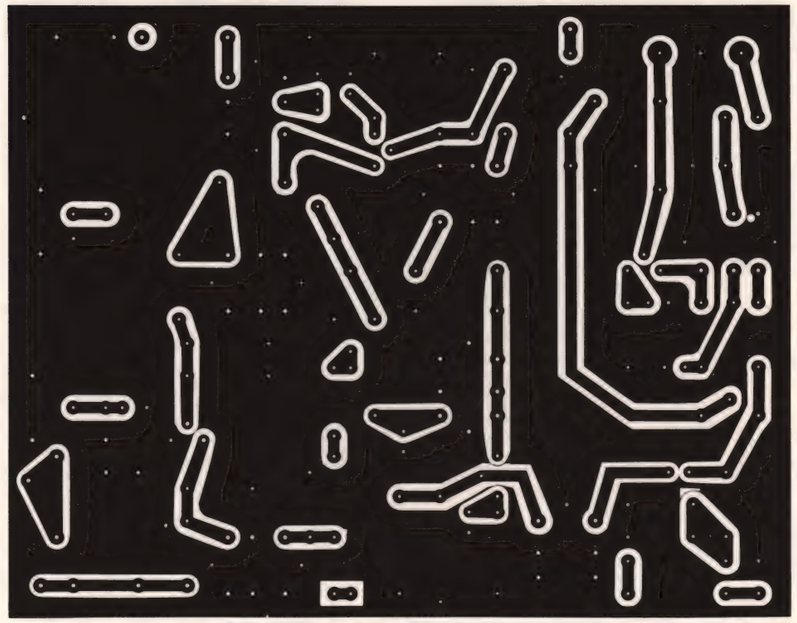


Fig.17 — Complete f.m. transmitter (high band, using BGY36)



(a)



(b)

Fig.18 — Printed-wiring board for module drive circuit (actual size):
(a) components side; (b) underside

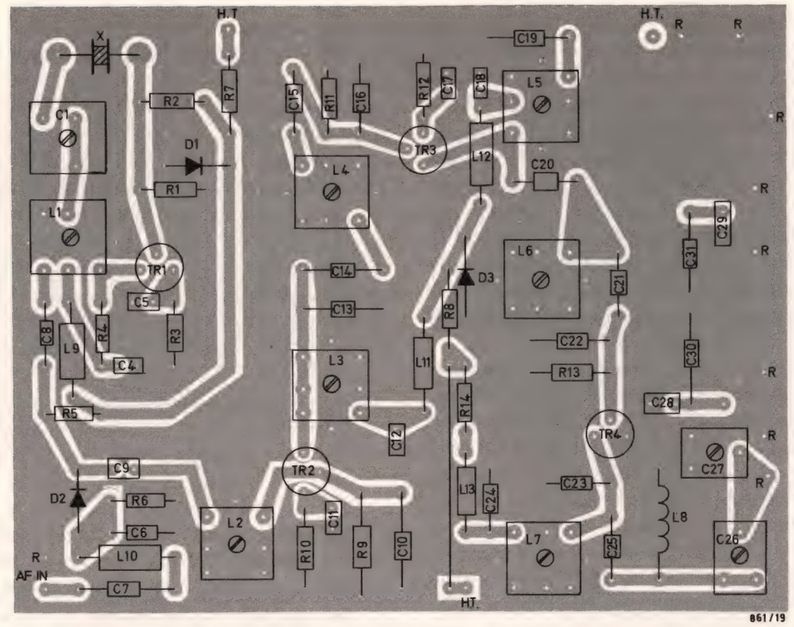


Fig.19 — Printed-wiring board layout

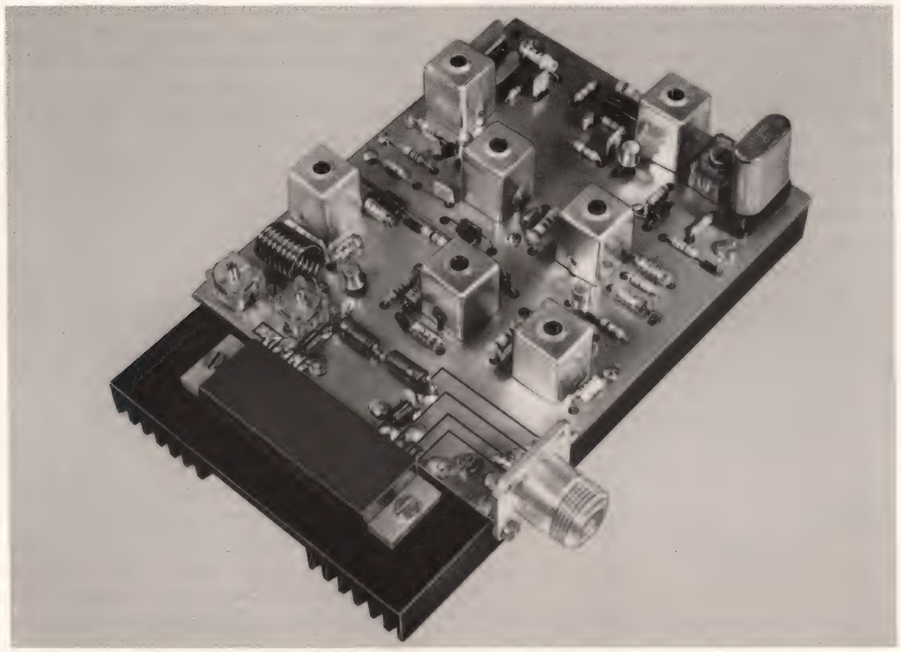


Fig.20 — F.M. transmitter using BGY32

sided copper-clad epoxy glass-fibre, with copper thickness of 300g/m² (1oz/ft²). Rivets, marked 'R' in Fig.19, are inserted to make ground connections between the upper and lower sides of the board. A small push-on heatsink should be used on the final doubler transistor TR_4. (This could be, for example, a Redpoint type 18F for the BSX19 or 5F for the 2N3866.)

OUTPUT FILTERING

To reduce the harmonic output from the module to a sufficient level to comply with statutory regulations regarding spurious signal output, additional filtering will be necessary at the module output.

In the U.K., at the present time, with a 25W transmitter the level of spurious radiation must not be less than −70dB. Thus, an additional −25 to −45dB attenuation is necessary in the output filter. This level can be achieved by using a three-section lowpass filter. For greater levels of harmonic rejection, additional sections may be necessary. If the in-band spurious signal rejection is insufficient, then it will be necessary to use a bandpass input or output filter: a bandpass filter at the module input is preferable. Measurements indicate that a lowpass output filter gives better stability than a bandpass output filter at high levels of output v.s.w.r. and at extremes of voltage and drive. As mentioned earlier, it is important to maintain a close 50Ω impedance match to achieve full power output.

It is desirable to drive the module from a resistive source. If the module is driven from a bandpass filter or tuned coupling network, then an attenuator with a loss of 1 to 3dB should be inserted between filter and module. This attenuator reduces any tendency to instability at low drive levels or low supply voltages, or due to mistuning of the input filter. A suitable π-section attenuator circuit is shown in Fig.21, and the appropriate components for various values of attenuation are given in Table 3.

The following guidelines are given to ensure good overall performance from a transmitter using the modules.

1. The driver unit should give a minimum r.f. output power of 180 to 250mW, with low spurious-signal content.

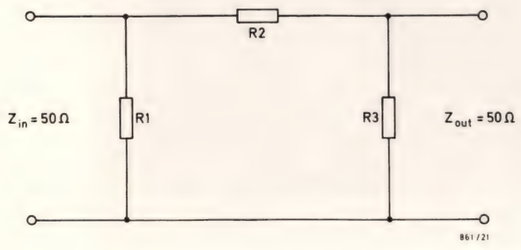


Fig.21 — Module input attenuator
(see Table 3 for component values)

TABLE 3

Resistor Values for Fig.21

Attenuation (dB)	$R_1 = R_3$ (Ω)	R_2 (Ω)
1.0	820	5.6
1.5	620	8.2
2.0	470	12
2.5	390	15
3.0	270	18

2. A tuned bandpass filter should follow the driver unit.
3. An attenuator (of approximately −3dB for the low-band or −1.5dB for the high-band modules) should be included between the bandpass filter and the module.
4. A lowpass filter should be included between the module and the aerial.

MISMATCHED LOADS

The effects of operating the modules with mismatched loads are shown in Figs.22 to 26. The Smith charts (Figs.22 to 25) and the curves of P_L against v.s.w.r. (Fig.26) are plotted up to a maximum value of output v.s.w.r. of 4. At higher values the modules may become unstable at certain phase angles of the mismatch.

From Figs.22, 24, and 26 it can be seen that the optimum load impedance is 50Ω resistive. Figs.23 and 25 show the module dissipation as a function of the load impedance.

TEST JIG

A suitable test jig for the modules is shown in Fig.27.

Type N connectors are used for the r.f. input and output on the jig; the module connections are made by means of a printed-wiring board. The board is 1.5mm (1/16in) epoxy glass-fibre, copper-clad on both sides to 600g/m² (2oz/ft²). The underside of the board is plain copper to act as a ground plane, and the connections on the components side are gold plated to avoid tarnish. A 2.5mm aluminium spacing plate under the board aligns the upper surface of the board with the module tags.

The width of the copper tracks which connect the module input and output tags to the Type N connectors is 2.5mm. This is, as described earlier, the correct width to give a microstrip transmission line of 50Ω characteristic impedance on a 1.5mm epoxy glass-fibre printed-wiring board.

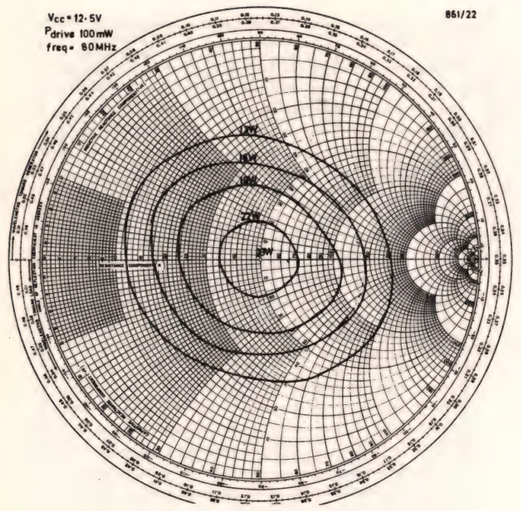


Fig.22 — P_L as a function of load impedance: BGY32
(V_s = 12.5V; P_D = 100mW; f = 80MHz)

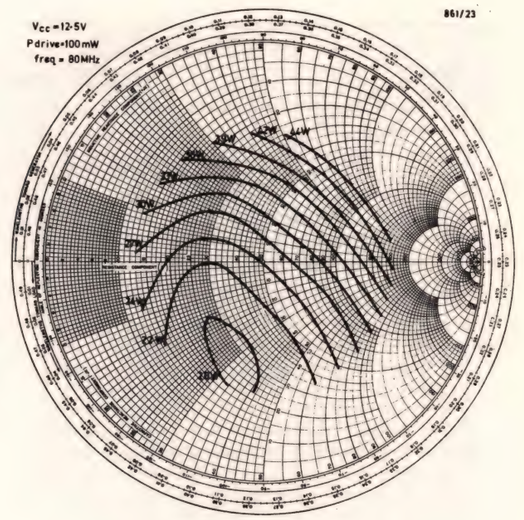


Fig.23 — Dissipation as a function of load impedance: BGY32
(V_s = 12.5V; P_D = 100mW; f = 80MHz)

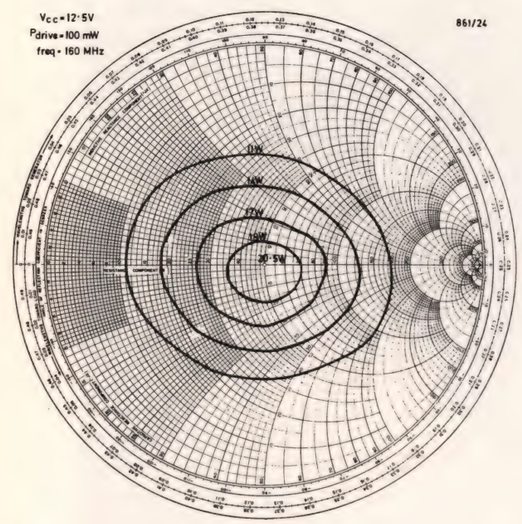


Fig.24 — P_L as a function of load impedance: BGY36
(V_s = 12.5V; P_D = 100mW; f = 160MHz)

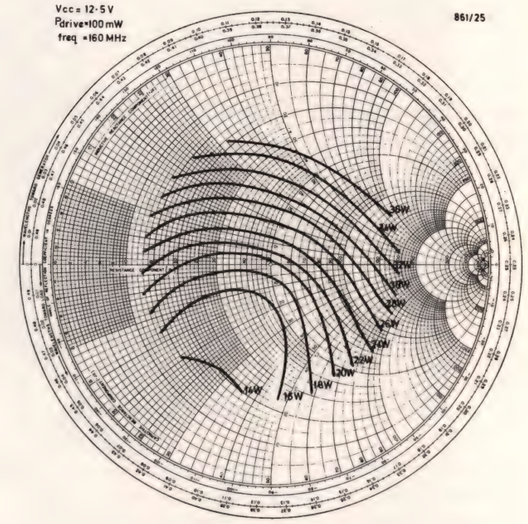


Fig.25 — Dissipation as a function of load impedance: BGY36
(V_s = 12.5V; P_D = 100mW; f = 160MHz)

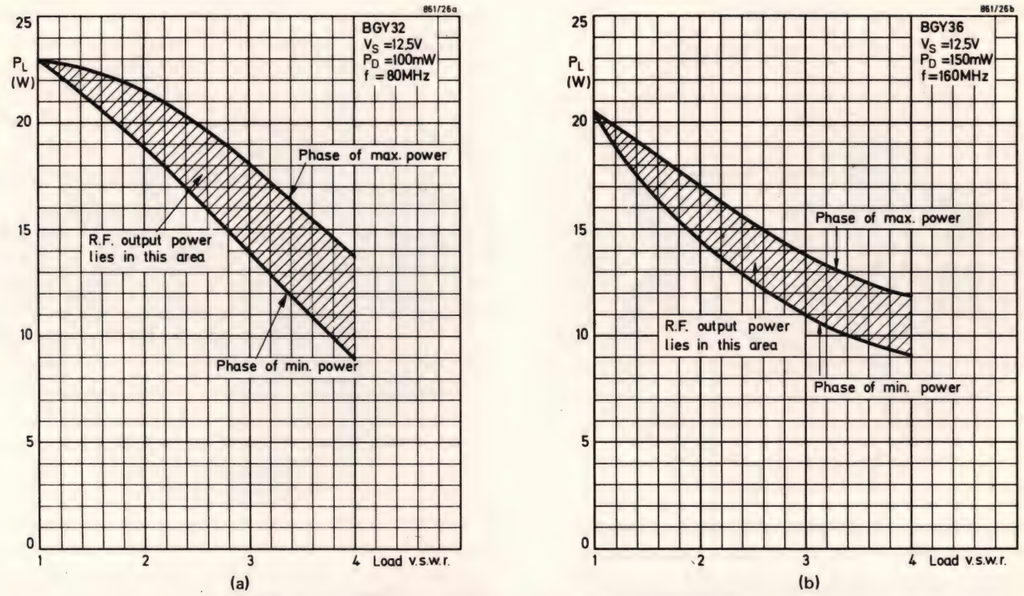


Fig.26 — Mismatch characteristics: (a) BGY32 (b) BGY36

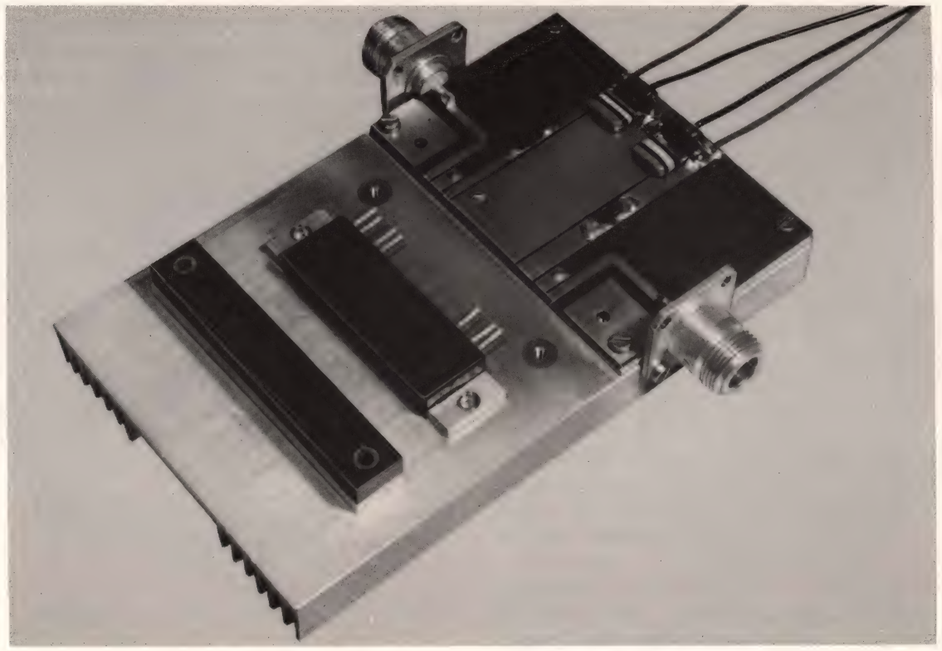


Fig.27a — Photograph of a test jig for the v.h.f. modules

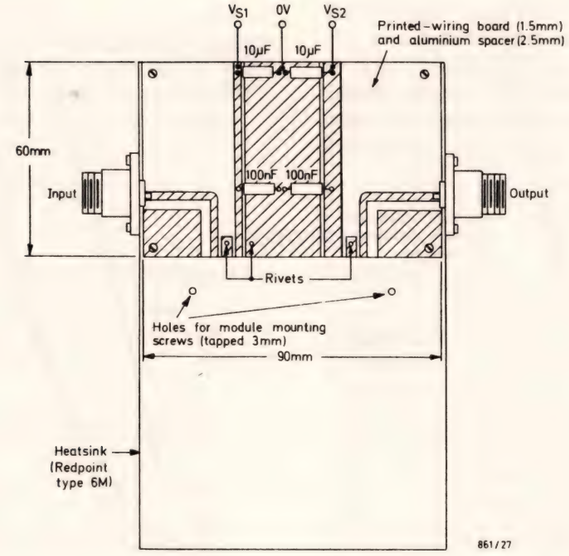


Fig.27b — Test jig for v.h.f. modules

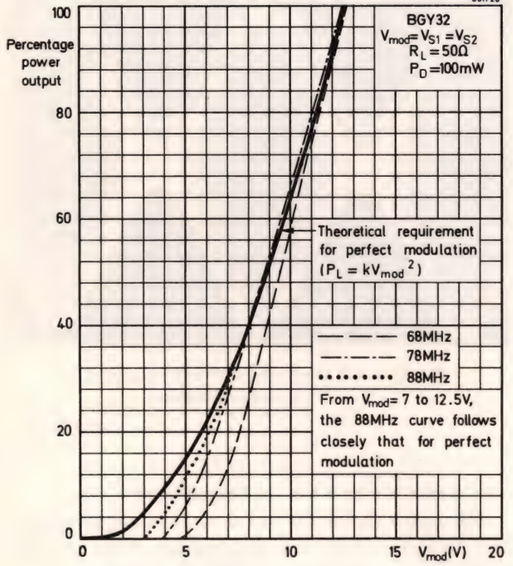


Fig.28 — A.M. characteristics of BGY32 (V_{S1} and V_{S2} modulated)

Ground connections on the upper side of the board are connected to the underside (ground plane) by small rivets. A p.t.f.e. clamping bar ensures good contact between the module tags and the printed-wiring board, without the need for soldering the tags.

A.M. OPERATION

The modules are designed for f.m. operation, but the possibility of amplitude modulation has been investigated. There are two simple methods of amplitude-modulating the output of a module:

1) modulating V_{s1} while V_{s2} is fixed;
2) modulating V_{s1} and V_{s2} together.

Fig.28 shows the effect of modulating both V_{s1} and V_{s2}, and Fig.29 shows the effect of modulating V_{s1} only, for the BGY32. The effects of both methods for the BGY36 are shown in Fig.30. On each graph the theoretical curve for perfect modulation is also plotted for comparison (perfect modulation is defined by the equation $P_L = kV_{mod}^2$).

The curves show that modulating both V_{s1} and V_{s2} together gives the better performance, with less distortion. The circuit of a series modulator, suitable for modulating V_{s1} and V_{s2}, is given in Fig.31. The 470Ω potentiometer R_2 sets the output voltage at zero modulation: it should be adjusted so that with no a.f. input, the modulated output voltage is half the module supply voltage (that is, 6.25V nominal).

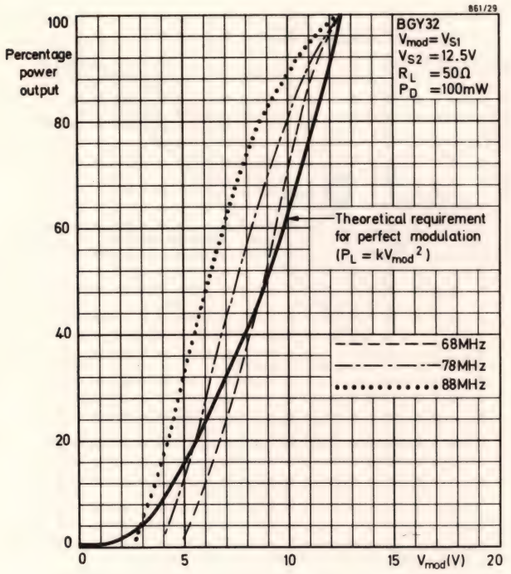


Fig.29 — A.M. characteristics of BGY32 (V_{s1} modulated)

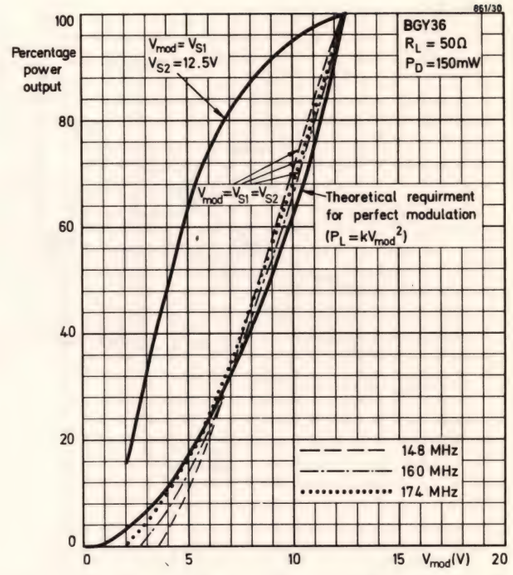


Fig.30 — A.M. characteristics of BGY36

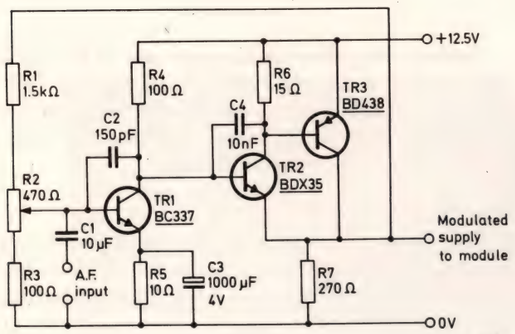


Fig.31 — Amplitude modulator for v.h.f. modules

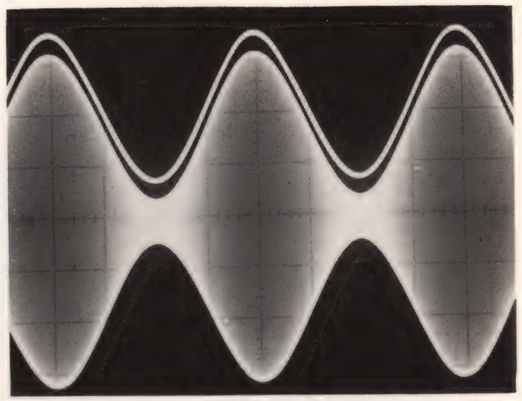


Fig.32 — A.F. input waveform and modulated r.f. output waveform

Fig.32 shows a typical modulated output waveform (BGY36) together with the modulator input, at 80% modulation depth. The distortion contributed by the modulator, at 80% modulation, is typically 2%. A carrier power level of 5W r.f. output can be obtained from either module, with distortion between 3 and 8%, at 80% modulation. Distortion varies with frequency, and there is considerable variation between samples of the modules. The BGY36 gives less distortion than the BGY32, and there is less distortion at high drive power (150 to 250mW). The a.m. performance of the other v.h.f. module variants has not been evaluated.

Although no instability was observed during laboratory investigations into the a.m. performance of the modules, it will be appreciated that modulating both V_{s1} and V_{s2} results in operation outside the published stability specification of the modules; that is, operation with supply voltage less than 10.5V. It is probable that, for guaranteed a.m. performance, selection would be necessary. Modulating V_{s1} only, which produces greater distortion, does result in operation within the stability specification.

INCREASED OUTPUT POWER

Higher output power can be obtained from a transmitter using the v.h.f. modules if an additional amplifier is used following the module. Details of suitable add-on amplifiers are given in Appendix 2.

FUTURE DEVELOPMENTS

This article describes application work on the current range of Mullard v.h.f. modules. Development work is in progress to extend this range of modules to cover a wider range of supply voltages, output power levels, and frequencies.

APPENDIX 1

Components List for Figs.16 and 17

Circuit reference	Fig.16	Fig.17
Resistors		
All resistors (except R_{15}) are Mullard CR25 series, ±5% tolerance.		
R_1	1.8kΩ	1.8kΩ
R_2	12kΩ	12kΩ
R_3	390Ω	390Ω
R_4†	4.7kΩ	5.6kΩ
R_5	39kΩ	39kΩ
R_6	8.2kΩ	8.2kΩ
R_7	220Ω	220Ω
R_8	120Ω	120Ω
R_9	560Ω	560Ω
R_{10}	120Ω	120Ω
R_{11}	560Ω	560Ω
R_{12}	39Ω	39Ω
R_{13}	560Ω	560Ω
R_{14}	39Ω	–
R_{15}	470Ω	470Ω
R_{16}	15Ω	4.7Ω

†May require adjustment depending on crystal activity.

Circuit reference	Fig.16	Fig.17
C_{10}	330pF (F)	150pF (F)
C_{11}	4.7nF (B)	2.7nF (B)
C_{12}	4.7nF (B)	2.7nF (B)
C_{13}	22pF (F)	12pF (F)
C_{14}	1.5pF (E)	1.5pF (E)
C_{15}	33pF (F)	18pF (F)
C_{16}	82pF (F)	47pF (F)
C_{17}	–	2.7nF (B)
C_{18}	2.7nF (B)	1.8nF (B)
C_{19}	33pF (F)	15pF (F)
C_{20}	1.5pF (E)	1.5pF (E)
C_{21}	56pF (F)	33pF (F)
C_{22}	120pF (F)	68pF (F)
C_{23}	100pF (F)	47pF (F)
C_{24}	12pF (F)	5.6pF (F)
C_{25}	1.5pF (E)	1.5pF (E)
C_{26}	57pF (A)	40pF (A)
C_{27}	57pF (A)	40pF (A)
C_{28}	22nF (C)	22nF (C)
C_{29}	22nF (C)	22nF (C)
C_{30}	10μF 25V (G)	10μF 25V (G)
C_{31}	10μF 25V (G)	10μF 25V (G)

Capacitors		
C_1	57pF (A)*	57pF (A)
C_2	82pF (F)	220pF (F)
C_3	–	47pF (F)
C_4	10nF (C)	2.7nF (B)
C_5	4.7nF (B)	2.7nF (B)
C_6	22nF (D)	22nF (D)
C_7	220nF (D)	220nF (D)
C_8	3.3pF (E)	1.5pF (E)
C_9	4.7nF (B)	3.9nF (B)

*Capacitor types:

A) 80908 series film dielectric trimmer
B) 630 series ceramic plate
C) 629 series ceramic plate
D) C280 series metallised film
E) Tubular ceramic; alternatively 632 series ceramic plate
F) Polystyrene; alternatively 632 series ceramic plate
G) 015 series electrolytic

Transistors

TR_1	BF115	BF115
TR_2	BC107	BC107
TR_3	BSX19	BSX19
TR_4	BSX19	2N3866
TR_5	BDX35	BDX35

Diodes

D_1	BZY88-C10	BZY88-C10
D_2	BA102	BA102
D_3	BZY88-C10	BZY88-C10

Coil winding details

Fig.16

L_1 43 turns, 0.16mm enamelled copper wire, tapped at 3 turns

L_2 70 turns, 0.16mm enamelled copper wire

L_3 22 turns, 0.4mm enamelled copper wire

L_4 22 turns, 0.4mm enamelled copper wire

L_5 8 turns, 0.45mm enamelled copper wire

L_6 8 turns, 0.45mm enamelled copper wire

L_7 5 turns, 0.45mm enamelled copper wire

L_8 8 turns, 1.0mm enamelled copper wire; i.d. 8.2mm; length 12mm

L_9 to L_{13} 3 turns, 0.4mm enamelled copper wire through FX1115 ferrite bead

Fig.17

L_1 30 turns,'0.14mm enamelled copper wire

L_2 34 turns, 0.16mm enamelled copper wire

L_3 15 turns, 0.4mm enamelled copper wire

L_4 15 turns, 0.4mm enamelled copper wire

L_5 4 turns, 0.4mm enamelled copper wire

L_6 4 turns, 0.4mm enamelled copper wire

L_7 3 turns, 1.0mm enamelled copper wire

L_8 3 turns, 1.0mm enamelled copper wire; i.d. 6.2mm; length 5mm

L_9 to L_{13} 3 turns, 0.4mm enamelled copper wire through FX1115 ferrite bead

L_1 to L_7 are close wound on Neosid 4mm formers with dust cores, enclosed in screening cans.

APPENDIX 2

Broadband Add-on Amplifiers

INTRODUCTION

To enable the power output of the v.h.f. modules to be increased, broadband amplifiers may be added to the transmitters described earlier. The amplifiers described in this Appendix will raise the power output of the transmitters to the 45 to 50W region.

The use of broadband techniques avoids the need to retune the transmitters over the operating frequency band of the modules. The amplifier for the BGY32 uses a BLY90 transistor to give 50W r.f. output over the 68 to 88MHz band; that for the BGY36 uses a BLW60 to give 45W r.f. output over the 148 to 174MHz band. In both cases the v.h.f. module is operated at reduced output power: this is achieved by reducing the driver stage supply voltage V_{s1}.

CIRCUIT DESIGN

The circuit of both amplifiers is shown in Fig.33. The single-stage circuit incorporates Chebychev lowpass impedance-transforming networks for input and output coupling, to give broadband performance.

The designed input and output impedance of the amplifier is 50Ω. Knowledge of the input and load impedances of the transistor is necessary to the design of the Chebychev networks; the impedances have been computed and are shown in Table 4.

The network component values have been calculated using standard tables (Ref.1). Computer investigation shows that a tolerance on each component value of ±5% should provide satisfactory reproduction of the performance of the prototype.

High-current capacitors, with low series inductance, must be used in the low-impedance sections of the coupling networks. Ordinary tubular ceramic or ceramic plate capacitors are not satisfactory: the prototype used good-quality porcelain chip capacitors.

Wideband decoupling across the supply rails prevents parametric instability. The base choke arrangement has been designed to prevent low-frequency instability.

CONSTRUCTION

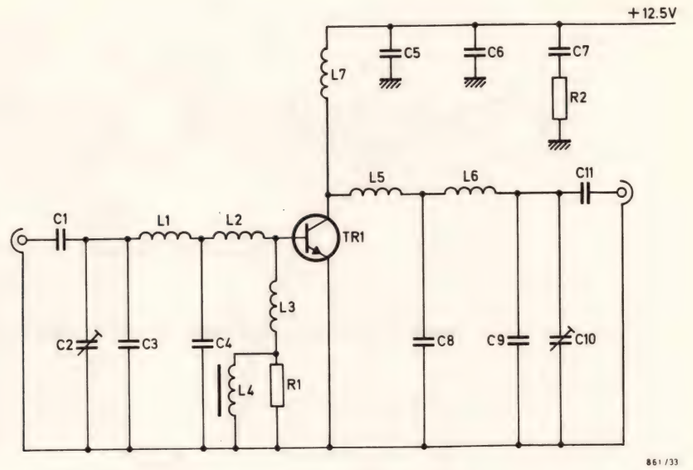
Printed-wiring boards for the two amplifiers are shown in Fig.34. The board material is Formica type CFG83, double-sided copper-clad epoxy glass-fibre board, with a copper thickness of 900g/m² (3oz/ft²). The underside of each board is plain copper to act as a ground plane: the upper and lower ground planes are connected by small rivets.

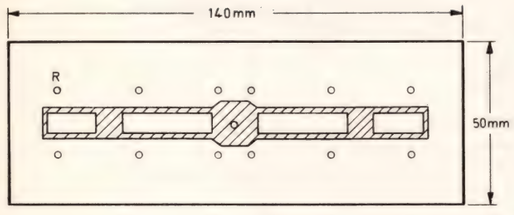
The board layouts are shown in Figs.35 and 36. To maintain the filter performance, component layout is critical: the positions of capacitors C_4 and C_8 are particularly critical.

Inductors L_2 and L_5 are fabricated directly on the printed-wiring board as shown in Figs.35 and 36. Certain other inductors (L_7 in the low-band amplifier; L_1, L_6, and L_7 in the high-band amplifier) are constructed from copper strip, cut to size and bent to shape as in Fig.37.

Components lists for the two amplifiers are given in Appendix 3.

Fig.33 — Circuit of add-on amplifiers





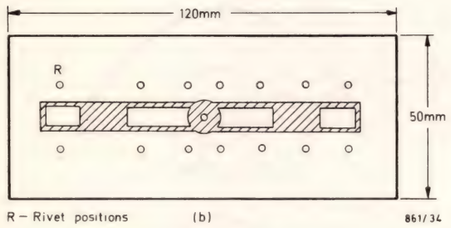


Fig.34 — Printed-wiring boards, shown for:
(a) low-band and
(b) high-band amplifiers
The shaded areas are etched

PERFORMANCE

The performance of the amplifiers is shown in Table 5, and in Figs.38a to 38d and 39a to 39d.

Figs.38a and 39a show the output power of the two amplifiers over the operating bandwidth; Figs.38b and 39b the load power as a function of drive power; Figs.38c and 39c the input v.s.w.r. against frequency; and Figs.38d and 39d the efficiency against frequency. Performance measurements are based on three samples of each amplifier.

Both amplifiers are stable with a load v.s.w.r. of 3:1, but some degree of instability at certain phase angles may occur with a v.s.w.r. of 5:1.

The harmonic output of the low-band amplifier at 68MHz is typically −35dB; that of the high-band amplifier at 148MHz typically −25dB. Harmonic output is reduced by a further 20dB at the high-frequency end of the operating band.

It is important that the amplifiers are not overdriven, particularly when operating into a high load v.s.w.r.

When the low-band amplifier is set to 50W output, or the high-band amplifier to 45W output, each amplifier is capable of surviving infinite mismatch without damage.

REFERENCE

1. MATTHAEI, G.I., Tables of Chebychev Impedance-transforming Networks of Lowpass Filter Form, **Proc. I.E.E.E.**, August 1964, pp.939 to 963.

TABLE 4

Input and Load Impedances

Transistor type	Frequency	R_i	X_i	R_L	C_L
BLY90	78MHz	1.67Ω	+j0.16Ω	2.0Ω	500pF
BLW60	160MHz	1.33Ω	+j1.0Ω	2.75Ω	190pF

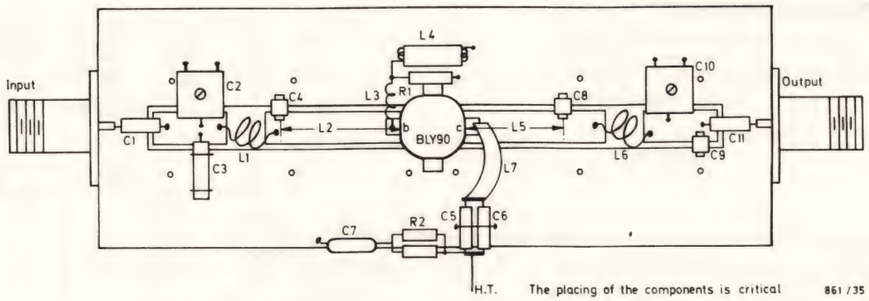


Fig.35 — Printed-wiring board layout for 50W low-band amplifier using BLY90

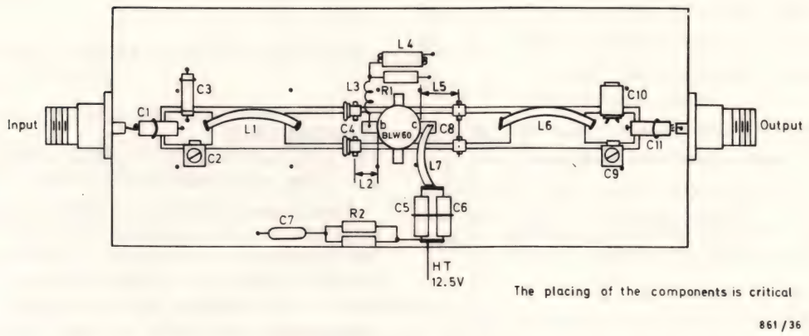


Fig.36 — Printed-wiring board layout for 45W high-band amplifier using BLW60

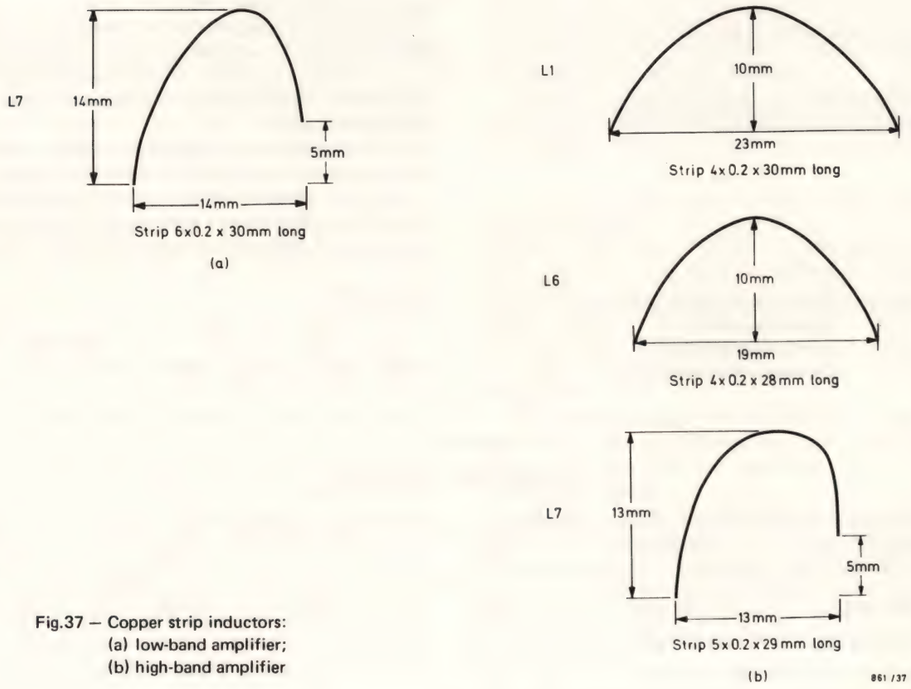
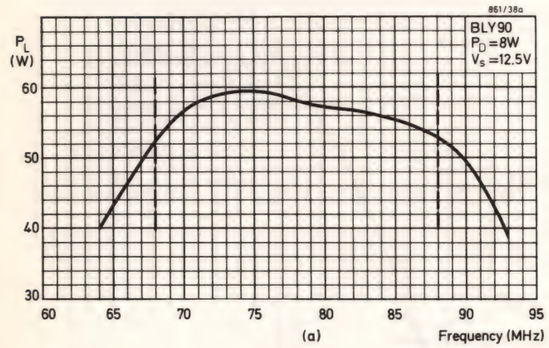
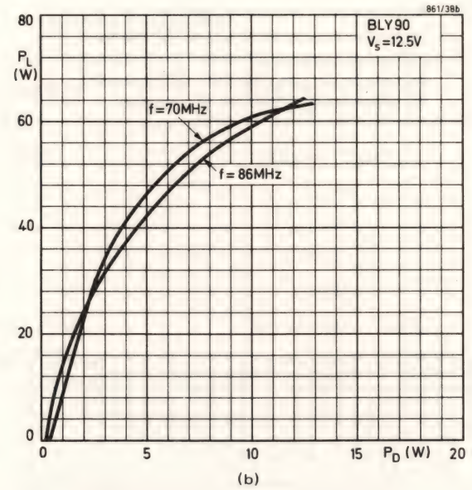
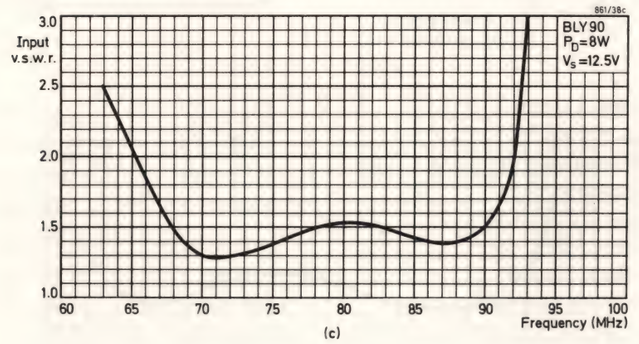


Fig.37 — Copper strip inductors:
(a) low-band amplifier;
(b) high-band amplifier

Fig.38 — Performance of low-band amplifier:
(a) output power as a function of frequency;
(b) output power as a function of drive power;
(c) input v.s.w.r. as a function of frequency;
(d) efficiency as a function of frequency







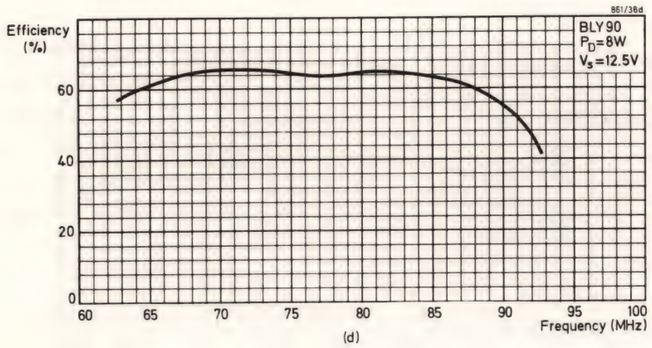
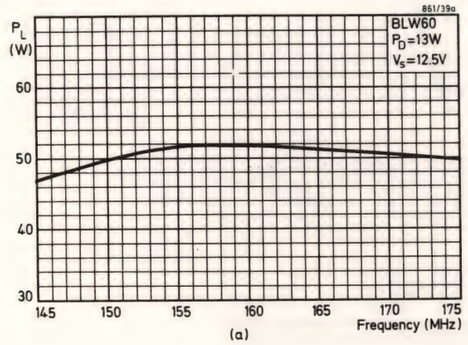
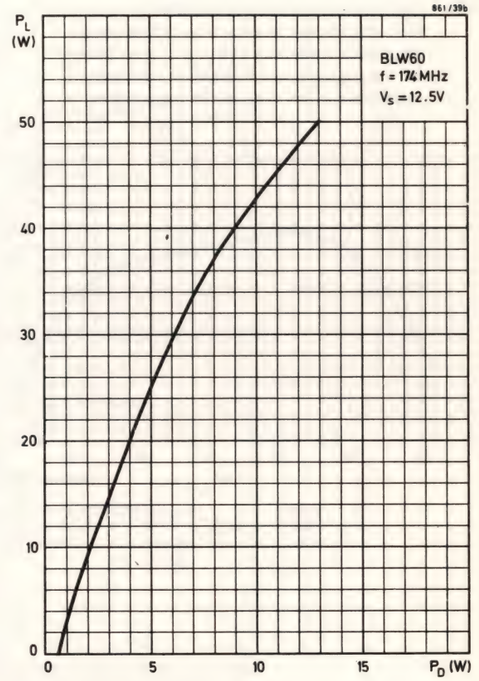


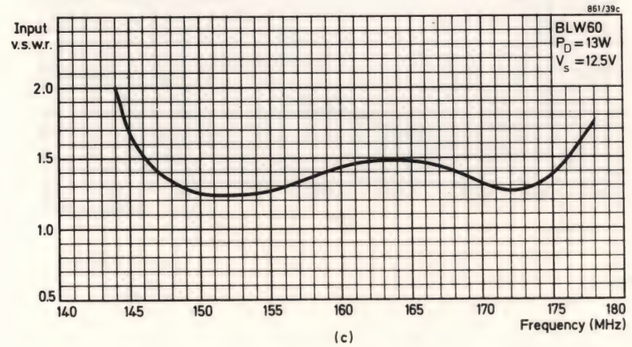
Fig.39 – Performance of high-band amplifier:
(a) output power as a function of frequency;
(b) output power as a function of drive power;
(c) input v.s.w.r. as a function of frequency;
(d) efficiency as a function of frequency



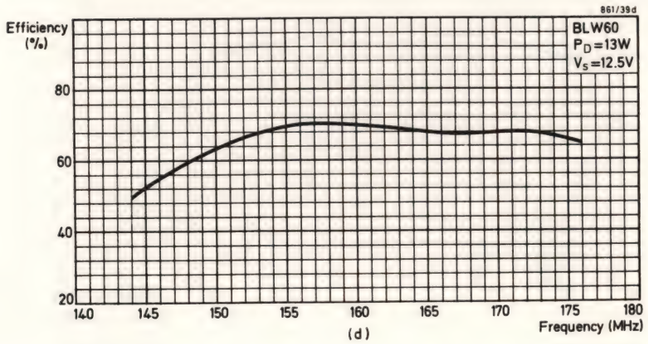
(a)



(b)



(c)



(d)

TABLE 5 **Amplifier Performance**

	Low-band amplifier	High-band amplifier
Frequency band	68 to 88MHz	148 to 174MHz
Supply voltage (nominal)	12.5V	12.5V
R.F. output power	50W	45W
Efficiency (typical)	65%	68%
Drive power	8W	13W
Harmonic output	Better than −35dB	Better than −25dB
Input v.s.w.r.	Less than 1.6:1	Less than 1.5:1

APPENDIX 3

Components List for Figs.35 and 36

Circuit reference	Fig.35	Fig.36
Transistors		
TR_1	BLY90	BLW60
Capacitors		
C_1	2.2nF (L)	680pF (L)
C_2	40pF (A)	18pF (M)
C_3	68pF (E)	33pF (E)
C_4	510pF (H)	2 X 150pF (J)
C_5	2.2nF (L)	1.5nF (L)
C_6	2.2nF (L)	1.5nF (L)
C_7	100nF (D)	100nF (D)
C_8	470pF (H)	2 X 82pF (H)
C_9	68pF (H)	30pF (K)
C_{10}	40pF (A)	18pF (M)
C_{11}	2.2nF (L)	680pF (L)

Capacitor types:

A) 80908 series film dielectric trimmer
B) 630 series ceramic plate
D) C280 series metallised film
E) Tubular ceramic NPO Philips 2222 555 series
H) ATC 100B, microstrip terminations, ±5%
J) As (H), in parallel with 2 X 15pF 632 series ceramic plate
K) Unelco J101 (mica), 350V, ±10%
L) Ceramic feedthrough capacitors Philips 2222 700 series
M) 80909 series film dielectric trimmer

Resistors

All resistors are Mullard CR37 series

R_1	10Ω	10Ω
R_2	2 X 10Ω in parallel	2 X 10Ω in parallel

Coil winding details

Fig.35

L_1	42.6nH	2 turns, 1.25mm enamelled copper wire, i.d. 8.3mm, length 10mm
L_2	7.8nH	(Fabricated on printed-wiring board – see Fig.35) length 26mm
L_3		9 turns, 0.45mm enamelled copper wire, i.d. 2.7mm, close wound
L_4		2.5 turns, 0.63mm enamelled copper wire through FX1898 ferrite bead
L_5	9nH	(Fabricated on printed-wiring board – see Fig.35) length 18.5mm
L_6	45nH	2 turns, 2mm enamelled copper wire, i.d. 9.6mm, length 10mm
L_7	35nH	(Copper strip – see Fig.37)

Fig.36

L_1	21nH	(Copper strip – see Fig.37)
L_2	2.4nH	(Fabricated on printed-wiring board – see Fig.36) length 4.4mm
L_3		8 turns, 0.45mm enamelled copper wire, i.d. 2.7mm close wound
L_4		2.5 turns, 0.63mm enamelled copper wire through FX1898 ferrite bead
L_5	6.1nH	(Fabricated on printed-wiring board – see Fig.36) length 8.7mm
L_6	26nH	(Copper strip – see Fig.37)
L_7	30nH	(Copper strip – see Fig.37)

Microwave doppler intruder alarms

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A microwave doppler alarm system for detecting intruders into protected areas is described. The radar unit is the Mullard CL8960 in one circuit or the CL8920 in an alternative circuit. Performance information is given.

INTRODUCTION

This article describes circuits which demonstrate the use of two Mullard X-band microwave doppler radar modules in intruder alarm applications. The modules are the CL8960 and the CL8920, and these were designed specifically for detecting movement of a remote target by monitoring doppler-shift in microwave radiation reflected from the target, and for application in intruder alarm systems.

The CL8960 comprises a Gunn oscillator cavity, which produces the energy to be radiated, mounted alongside a mixer cavity which mixes the reflected energy with a sample of the oscillator signal. The module is fully described in Ref.1. The CL8920 contains a microwave integrated circuit (MIC). Microwave energy generated by a Gunn oscillator is radiated via a circulator; reflected energy returns to the same port of the circulator, and is passed to a mixer diode together with a reference sample of the oscillator signal. A varactor diode controls the frequency of the oscillator and is used for setting the centre frequency. Both the CL8960 and CL8920 are self-contained: only a power supply circuit and an amplifier need be added to construct a complete intruder detector system.

Any object within the radiation field of a module will reflect a proportion of the radiated energy back to the module. If the object is stationary, then the reflected signal is at the same frequency as the transmitted signal: the output from the mixer is a d.c. voltage dependent on the relative phase of the transmitted and reflected signals.

When a signal is reflected from a moving object, however, the relative phase of the transmitted and reflected signals will vary with the rate of movement, and a difference frequency is produced (the doppler effect). The mixer output will then be an a.c. voltage, the frequency of which will depend on the relative velocity of the moving object. For the CL8960 and CL8920 modules, the transmitted frequency is 10.7GHz, and the output (doppler) frequency is approximately 31Hz for every 1mph (0.45m/s) of relative velocity between object and module. Thus for velocities up to about 400mph, the output frequency is within the audible range, and for this reason the output of the module is referred to as the a.f. output.

The a.f. output can be used in many ways for movement indication, measurement of speed or distance, etc.. This article deals with the application of the CL8960 (Fig.1) and CL8920 (Fig.2) in intruder alarm systems. Consideration is first given to the design of the doppler signal processing system.

INTRUDER ALARM DESIGN

Fig.3 is a block diagram of a typical motion detection system using a CL8960 or CL8920 doppler radar module. The a.f. output from the CL8960 or CL8920 is amplified, filtered to give the required bandwidth, and is then used to trigger the output unit which in the case of an intruder detector system would probably be an audible alarm. The discriminating circuit ensures that the system responds only to the desired input as far as possible. The

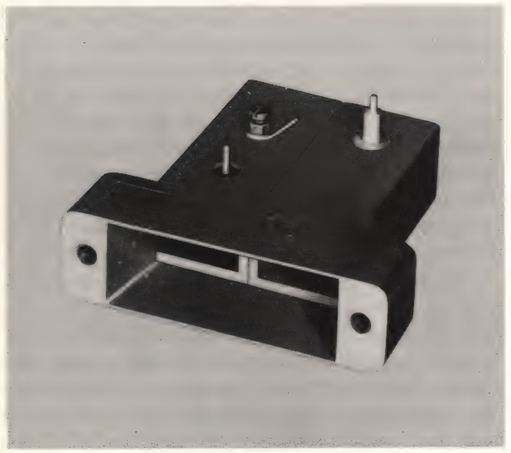

Fig.1 – CL8960 doppler radar module

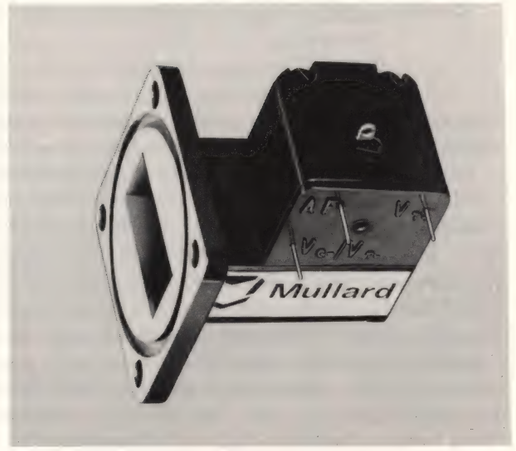

Fig.2 – CL8920 doppler radar module

circuit described later is arranged so that the output is triggered only when an amount of doppler energy is received in a given time, and not when the same amount of energy arrives little by little.

The design approach associated with processing circuits for intruder detector systems is largely subjective. Whilst the function of the circuit is to detect the presence of an unwanted intruder, it is also of prime importance to eliminate the possibility of a false alarm. To fulfil the latter requirement the location and on-site adjustment of the equipment are at least as important as the circuit design.

The system design engineer will need to consider the two possible causes of false alarms:

1) system-generated or internally-generated noise;
2) externally-generated energy.

System noise

For the module to achieve its maximum useful range whilst giving adequate immunity against false alarms, the correct signal-to-noise ratio must be established and maintained. The signal level is fixed by the Gunn output power, the two-way path loss, the target radar cross-section, and the mixer conversion loss; scope for further improvement therefore exists only in controlling the output noise level, the main contributions to which are as follows.

Noise and ripple on the Gunn bias power supply will cause modulation of the frequency and amplitude of the oscillator output, which in turn will modulate the signal at the mixer diode. Noise and ripple on the mixer bias supply will have a similar effect. Effective smoothing of the bias supplies is therefore imperative.

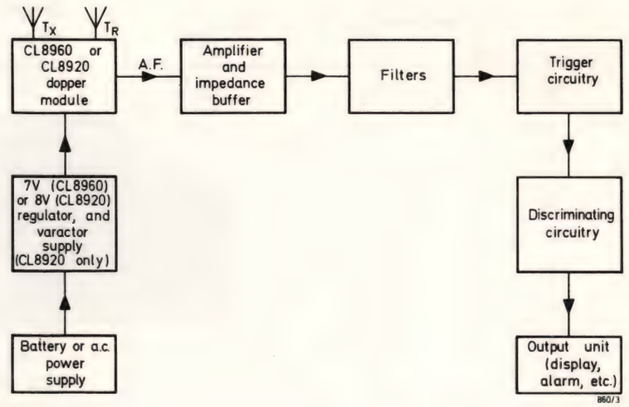

Fig.3 – Block diagram of motion detector system using CL8960 or CL8920

Microwave energy from the doppler module can be absorbed by components, such as diodes, in the processing circuit. Where the module and the processing circuit are enclosed in the same housing, the processing circuit should be protected by a coating of an appropriate microwave-absorbent material.

Amplifier noise added to the signal during processing could be minimised by matching the module into an amplifier with a low input impedance (approximately 2kΩ). The input stages of the amplifier should then use low-noise components. The overall noise figure of the amplifier and processing circuitry, referred to the amplifier input, should, in this case, be 2μV maximum in a bandwidth between 1Hz and 1kHz.

An alternative arrangement is shown in Fig.4 where the optimum mixer d.c. bias is derived from a potential divider and the mixer a.f. output is fed via a coupling capacitor to a high input impedance amplifier (Z_{in} > 100kΩ). Because of the impedance mismatch, a degradation in signal-to-noise performance will occur, but in this case a constant amplifier gain will be obtained over a range of modules. It will, however, be necessary to provide adjustable gain facility for setting up constant amplifier output voltage to accommodate variations in range, target cross-section, and voltage sensitivity of different modules.

This arrangement (Fig.4) is the one most commonly used by equipment manufacturers, and has therefore been adopted for data characterisation on the CL8960.

Table 1 shows the difference in signal-to-noise ratio obtained from the high and low input impedance amplifiers for a random sample of CL8960 operated with

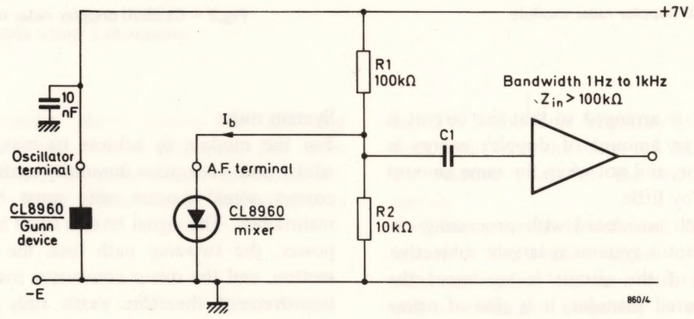

Fig.4 — Circuit used for obtaining CL8960 performance figures

TABLE 1

Comparison of High and Low Impedance System

Unit	High Z $\frac{S+N}{N}$ (dB)	Low Z $\frac{S+N}{N}$ (dB)
A	30.6	31.5
B	50.0	60.1
C	32.3	34.7
D	54.0	58.3
E	22.5	23.6
F	31.7	42.0
G	15.2	15.3
H	32.0	37.6
I	19.3	25.2

35μA d.c. bias and −19dBm L.O. power. These signal-to-noise ratios are for a fixed input signal (9 randomly selected units).

Externally-generated noise

Noise from external electromagnetic radiation can be minimised by enclosing the module in a metal housing.

The module will respond to fluorescent a.c. lighting in the target area, because the ionised gas acts as a modulated reflecting target during discharge, and so a signal at twice the mains frequency appears at the detector. If the light fittings cannot be shielded then a 100Hz notch filter should be included in the a.f. processing circuit. Alternatively a fan-antenna can be employed to give a wide beam in the horizontal plane with a narrow vertical beamwidth, thus avoiding reflections from the light fitting.

Other possible causes of external noise, and therefore false alarms, are: vibration due to heavy vehicles which can cause the rigidly-mounted intruder alarm to move

relatively to other reflecting surfaces in the room; air turbulence in plastic water-pipes; movement of suspended objects, etc.

Bandwidth

Most of the noise sources outlined above give a broad noise spectrum, and their effects can be significantly reduced by the introduction of filters to limit the amplifier bandwidth. As stated earlier, the frequency of the doppler output is approximately 31Hz per mph of target speed.

On first consideration, a processing circuitry passband centred on 120Hz might be thought desirable, as this would give a maximum response at medium walking pace. However, the majority of existing alarm systems use amplifiers with a peak response at about 20Hz, the signal being attenuated at frequencies above 40Hz and below 5Hz.

The reason for this choice of passband is the fact that both hesitant movement, and the limb and torso movements associated with regular walking, produce velocity variations which pass through zero. Thus, doppler frequencies from zero upwards are produced. It has been found that a man target moving at slow walking pace axially towards or away from the microwave radiating antenna generates a doppler frequency spectrum centred at about 50Hz. Similar movement at right angles to the antenna axis produces a spectrum from about 5 to 15Hz.

Protected volume

An ideal intruder alarm would give complete protection throughout a well-defined volume, and have zero response to movement outside that volume.

Fig.5 illustrates the requirements of a practical system: there are three nested volumes A, B, and C. The system must always give an alarm in response to movement inside volume A (*protected zone*), and never to movement outside volume C (*free access zone*). In practice, of course, the volumes will not be regular in shape because of the fan-shaped radiation pattern of the microwave modules.

The target gain G_T of an object is defined by:

$$G_T = 10 \log_{10} \left(\frac{4\pi\sigma}{\lambda^2} \right) \text{ dB}, \qquad \ldots (1)$$

where σ, the radar cross-section, is approximately frequency-independent provided that the target is large compared with the wavelength λ. Eq.1 is plotted for X-band frequencies in Fig.6, and it can be seen that the radar cross-section of a man target is taken as approximately 1m², which corresponds with a target gain of 42dB. It has been found, however, that the actual radar cross-sections of persons vary between 0.1 and 2m²; from Fig.6, therefore, the equivalent X-band target gain can vary between 32 and 45dB. This variation gives rise to the *zone of uncertainty*, shown in Fig.5 as volume (B-A).

The volume (C-B) in Fig.5 is the *safety factor zone*, where target movement will not induce a response. The volume C may represent a total warehouse space with the other two zones within it.

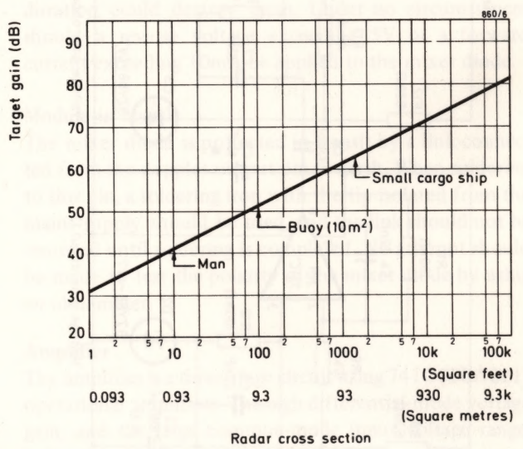

Fig.6 — Target gain versus target size

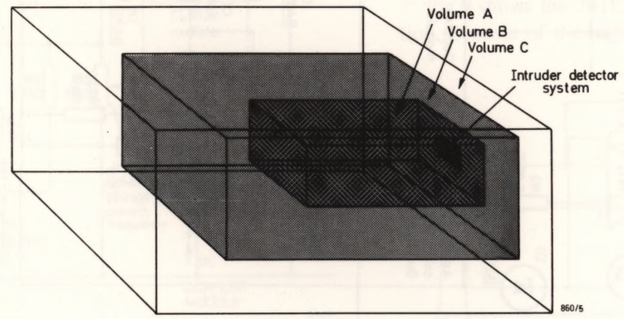

Fig.5 — Zones associated with intruder detector (theoretical)

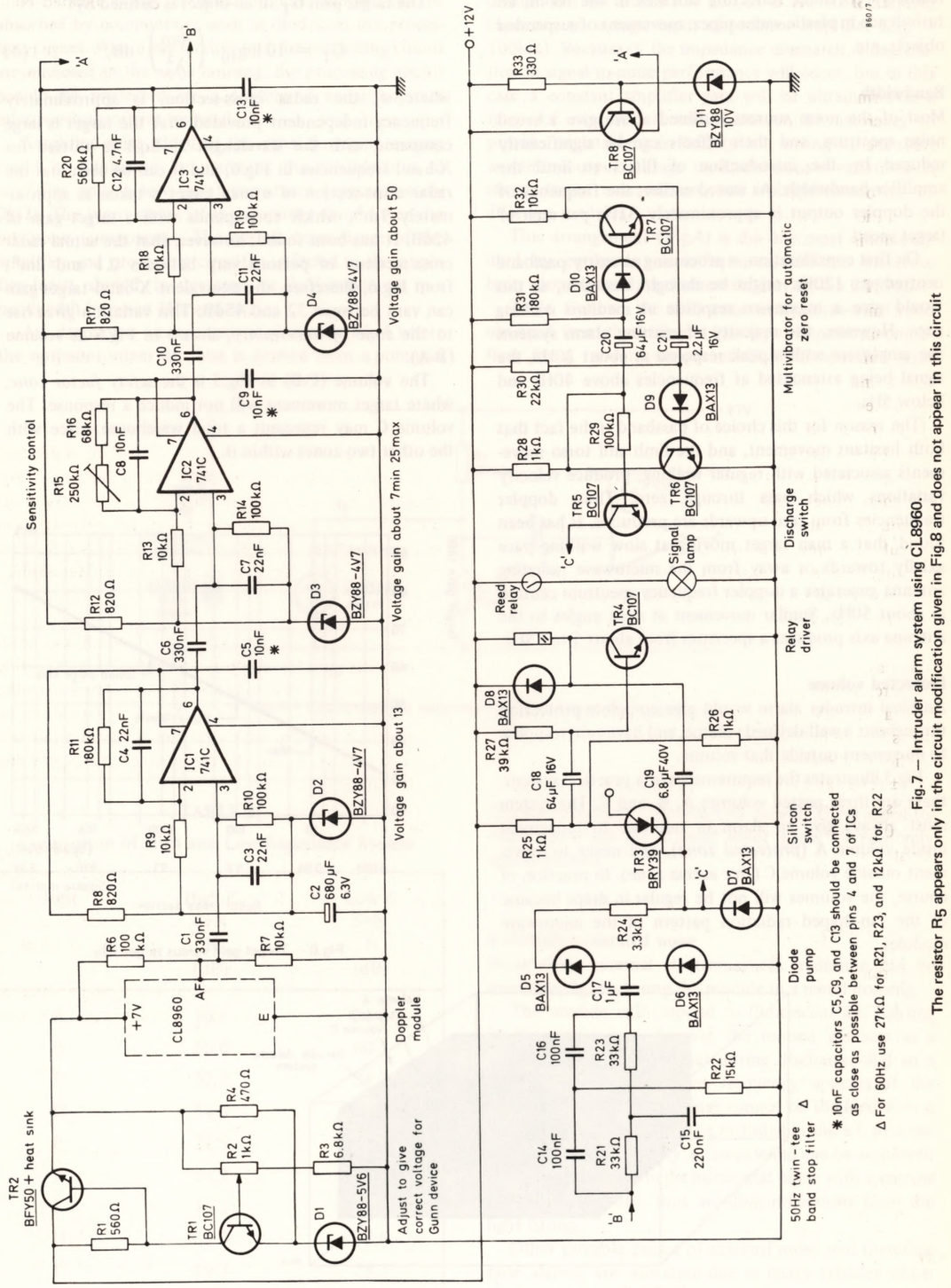

Fig.7 — Intruder alarm system using CL8960.

PROCESSING CIRCUITS FOR INTRUDER ALARMS

Two distinct types of signal-processing circuits are commonly used in intruder detector and alarm systems. The energy-integrating type of circuit operates after a predetermined amount of energy has been received from the microwave module a.f. output; the pulse-counting type operates after the a.f. output signal has reached a predetermined threshold level a certain number of times. The processing circuit adopted to demonstrate the capabilities of these modules is of the energy-integrating type and is described below.

CIRCUIT DESCRIPTION

The demonstration circuit, is shown in Figs.7 and 8. The a.f. signal from the CL8960 (Fig.7) or CL8920 (Fig.8) passes through an amplifier (with peak response at about 12Hz) and a twin-tee bandstop filter centred on the mains frequency, and is applied via a diode pump to the trigger of a silicon controlled switch. If the energy present in the amplified signal is sufficient to operate the switch, then a pair of relay contacts open for about 1s, and then close again, simulating the resetting of the system. This action is repeated if the energy is still present. To prevent unwanted actuation of the relay resulting from a slow build-up of energy from noise, the trigger of the SCS is shorted to the 0V line approximately every five seconds.

Power supply

The circuits of Figs.7 and 8 are both designed to operate from a 12 ± 2V supply, and differ only in the arrangements for the biasing of the microwave modules.

The CL8960 requires a Gunn supply voltage of +7.0 ± 0.1V, at a current of typically 140mA. The series stabiliser shown in Fig.7 gives a Gunn voltage of 7.0 ± 0.08V when operated from 12 ± 2V, with an adjustment range from 6.6 to 7.6V.

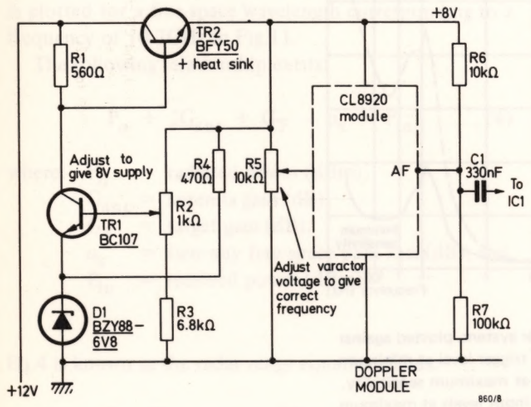

Fig.8 — Circuit modifications for use with CL8920

Fig.8 shows only the CL8920 and associated components, because the remainder of the circuit is the same as that of Fig.7. The CL8920 Gunn supply voltage is 8.0 ± 0.2V, and is set by adjusting the 1kΩ potentiometer R_2. The bias for the tuning varactor is between 1 and 12V, with a maximum current of 25μA, and is set by adjusting R_5 to give the specified operating voltage.

Bias supply

To optimise the sensitivity and noise performance of the doppler module, the mixer diode must be biased by reflected local oscillator coupled power and an externally-applied d.c. bias current. The sum of these should be approximately 42μA, normally consisting of 35μA of d.c. bias and the remainder from the local oscillator; the exact amount of the latter may depend upon the material used for the microwave window (radome).

Care of module

The mixer and Gunn bias supplies should be stable and protected against transients. Both the diodes are of low junction capacitance, and a transient even of very short duration could destroy them. Under no circumstances should a reverse voltage exceeding 5V or a forward current exceeding 10mA be applied to the mixer diode.

Module in transit

The mixer diode is protected in transit by a link connected from the doppler output pin to earth. When soldering to this pin, a soldering iron with the tip isolated from the mains supply should be used, and the link should not be removed until soldering is completed. No attempt should be made to test the polarity of the mixer diode by using an ohm-meter.

Amplifier

The amplifier is a three-stage circuit using 741C (TBA221) operational amplifiers. The high differential-mode voltage gain, and the large common-mode input voltage range, make the 741C particularly suitable for use as a non-inverting amplifier: this is the configuration in which it is used in the present circuit.

Fig.9 shows the 741C in the non-inverting configuration. Because of the high input impedance and very low

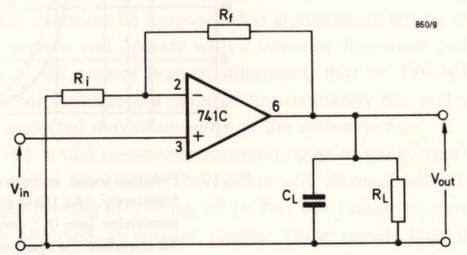

Fig.9 — 741C (TBA221) in non-inverting configuration

output impedance (<1Ω), low-value non-electrolytic coupling capacitors can be used between stages. The voltage gain of the amplifier in Fig.8 is given by:

$$G_V = \frac{R_f + R_i}{R_i}, \qquad \ldots (2)$$

and the amplifying section of the circuit of Fig.7 would have a maximum gain of approximately 32 000. However, the use of coupling and feedback capacitors to obtain the desired frequency response causes a considerable reduction in gain. The mid-band overall gain of the amplifier has been measured as 16 600 at the maximum setting of the sensitivity control, and 4450 at minimum sensitivity.

If a higher gain were required, it could be achieved by increasing the value of one or more of the feedback resistors, and reducing the associated parallel capacitor to maintain the same impedance.

The three 741C operational amplifiers are operated from a single stabilised supply, an artificial common line being created for each one by a voltage reference diode. It may be preferable to eliminate the 15mA current drain of the diodes by using a symmetrical power supply to provide the more usual common 0V line.

The frequency response of the amplifier itself is not given, because it is modified by the behaviour of the triggering circuit. Triggering occurs as the result of charge build-up in a capacitor; since the charging period is fixed, high-frequency signals will convey more charge in a given time than low-frequency signals of the same amplitude. The normalised input levels which will just cause triggering are plotted against frequency, at maximum and minimum gain settings, in Fig.10.

The 5:1 bandwidth is between 3 and 32Hz at minimum gain, and between 4 and 24Hz at maximum gain.

Filters

The 50Hz twin-tee bandstop filter gives a voltage loss, at the peak of its response, of about 50%. In the demonstration circuit the filter components were of normal tolerance and, as can be seen from Fig.10, the 'notch' occured at about 46Hz.

For use with 60Hz mains, the filter response may be modified by using 27kΩ resistors instead of 33kΩ, and 12kΩ instead of 15kΩ.

The circuit does not incorporate a 100Hz notch filter as a precaution against the effects of fluorescent lighting because the response of this amplifier circuit is sufficiently low at 100Hz.

Relay switching circuit

Under quiescent conditions, the relay driver transistor TR_4 is conducting, the relay contacts are closed, and the signal lamp is lit. In the presence of a doppler signal, the diode pump D_5 D_6 charges the 6.8μF capacitor C_{19} connected between the cathode gate of the silicon switch TR_3 and the collector of TR_4. A sustained 10Hz signal of 600mV peak value at the bandstop filter output will charge the capacitor in about 2s.

When the capacitor is charged, TR_3 conducts, the relay driver transistor TR_4 is switched off, and the signal lamp goes out. Because of a monostable action, TR_4 is switched on again, and the relay reset, after about one second. This switching cycle is repeated if the doppler signal is still present. In a practical system, the alarm state indicator (signal lamp) would be remote from the intruder alarm and the relay would be reset by the security authority.

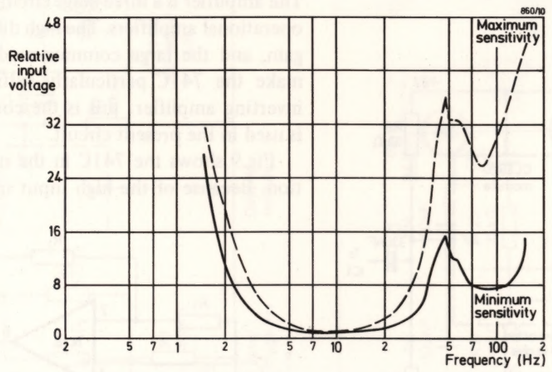

Fig.10 – Relative input voltage to trigger system, plotted against frequency. (At 10Hz the input trigger level at minimum sensitivity was 7.7 times that at maximum sensitivity. To compare the responses, the input levels at maximum sensitivity have therefore been multiplied by 7.7)

As previously mentioned, to avoid unwanted alarms due to charge build-up under quiescent conditions, the input of the silicon switch is periodically discharged to zero. This is achieved by transistor TR_5, which conducts for about 100ms every 5.5s, being driven by the multivibrator TR_6/TR_7.

CIRCUIT PERFORMANCE

Using a 10Hz sinewave input to determine the performance of the amplifier and trigger circuit, it has been found that the minimum value of input signal which will activate the alarm is 215μV r.m.s. with the sensitivity control at minimum, and 57μV r.m.s. with maximum sensitivity.

SYSTEM PERFORMANCE

The intruder alarm system has been tested in a room with a minimum of metal reflecting objects. The target used was a hollow copper sphere, freely suspended by a nylon line. Movement was instigated by jerking a long nylon line attached to the sphere, from a position well out of range.

The diameter of the target sphere was 35cm, and so its radar cross-section was $0.1m^2$. This is the minimum value to be expected for a man target, and corresponds to a target gain of approximately 32dB (see Fig.6).

For the circuit of Fig.7, using the CL8960 module with the standard 5dB antenna supplied, the alarm was just activated at a range of 4m when the processing circuit was set to minimum sensitivity.

The two-way free-space path loss is given by

$$a_s = 40 \log_{10} \left(\frac{4\pi D}{\lambda}\right) \text{dB}, \qquad \ldots (3)$$

where D is the range and λ the wavelength. This equation is plotted for a free-space wavelength corresponding to a frequency of 10.7GHz in Fig.11.

The following relationship exists:

$$P_o + 2G_{ant} + G_T - a_s = P_{in}, \qquad \ldots (4)$$

where: P_o = radiated power (dBm);
G_{ant} = antenna gain (dB);
G_T = target gain (dB);
a_s = two-way free-space path loss (dB); and
P_{in} = received power (dBm).

Eq.4 is known as the radar range equation. Thus:

$$P_o - P_{in} = a_s - 2G_{ant} - G_T, \qquad \ldots (5)$$

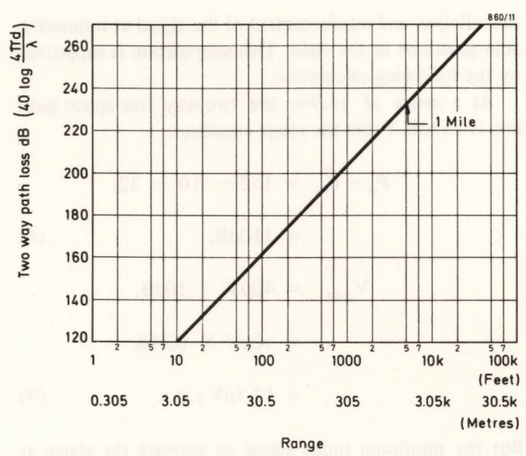

Fig.11 – Two-way free-space path loss

and for the present system:

$$P_o - P_{in} = 128 - 10 - 32,$$
$$= 86\text{dB}. \qquad \ldots (6)$$

From the CL8960 published data, the typical a.f. output voltage for an input power 100dB down on the output power is 40μV. In the present case the input power is only 86dB down on the output power, and so:

$$V_{out} = 40\mu V + 14\text{dB}$$
$$\simeq 40\mu V \times 5$$
$$= 200\mu V \text{ r.m.s.}$$

(The measured value of the minimum input voltage at the processing circuit to activate the alarm is, as stated earlier, 215μV.)

Again from the data, the minimum (S + N)/N is 18dB for a typical output of 40μV when the input power is 100dB down on the output power. With an input power 86dB down on the output power, therefore, the system (S + N)/N ratio is 32dB.

The power gain of the amplifier at maximum sensitivity is 11.5dB greater than that at minimum sensitivity. It may therefore be supposed that at maximum sensitivity the system will operate with a two-way free-space path loss 1.5dB greater than at minimum, that is, 139.5dB. This corresponds to a range of approximately 8m, and so the expected maximum range of the system is 8m.

The actual measured maximum range of the system is somewhat uncertain. The system still alarmed with the target moving at a range of 16.9m, but failure to alarm was observed at smaller ranges. These results indicate that a field standing-wave pattern existed, giving rise to

cancellation and reinforcement of the signal at unpredictable positions in the field. This supposition is supported by the following calculation.

At a range of 16.9m, the two-way free-space path loss is 152dB. From the range equation:

$$P_o - P_{in} = 152 - 10 - 32,$$

$$= 110\text{dB}; \quad \ldots(8)$$

$$V_{out} = 40\mu\text{V} - 10\text{dB},$$

$$= 40\mu\text{V} \times 0.316,$$

$$= 12.7\mu\text{V r.m.s.} \quad \ldots(9)$$

But the minimum input signal to activate the alarm at maximum sensitivity is 57μV r.m.s., and therefore the measured range of 16.9m is artificially high.

Using the measured value of maximum amplifier sensitivity to calculate the theoretical maximum range, gives a value of 8m. The theoretical minimum range calculated by the same method agrees well with the measured value. The discrepancy between measured and calculated values of maximum range can be accounted for by assuming that multiple reflections occurred from the vinyl floor tiles inside the measurement building.

False alarms

No false alarms occurred when the system was operated continuously for 65 hours, with the sensitivity control at maximum, with the microwave energy being absorbed by a graphite-loaded polystyrene foam tile having a re-entrant face.

It must be remembered that the system cannot distinguish between, say, a man target moving at long range and a much smaller object at close range, with similar equivalent target gain. The installation engineer should therefore take precautions against small animals, etc., approaching close to the doppler module. Winged insects have been accused of causing false alarms; it seems reasonable to suggest that an insect repellent be used within the protected area if this problem is likely to arise.

As mentioned previously, false alarms can be caused by the presence of fluorescent lamps in the area to be protected. Due regard must also be paid to objects which will move with air currents: this includes curtains, venetian blinds, and flexible walls, roofs, or doors etc. Careful siting of the intruder alarm system is therefore most important.

REFERENCE

1. CL8960 X-band doppler radar module, Technical Information 6, TP1480/1, Mullard Limited, 1975.